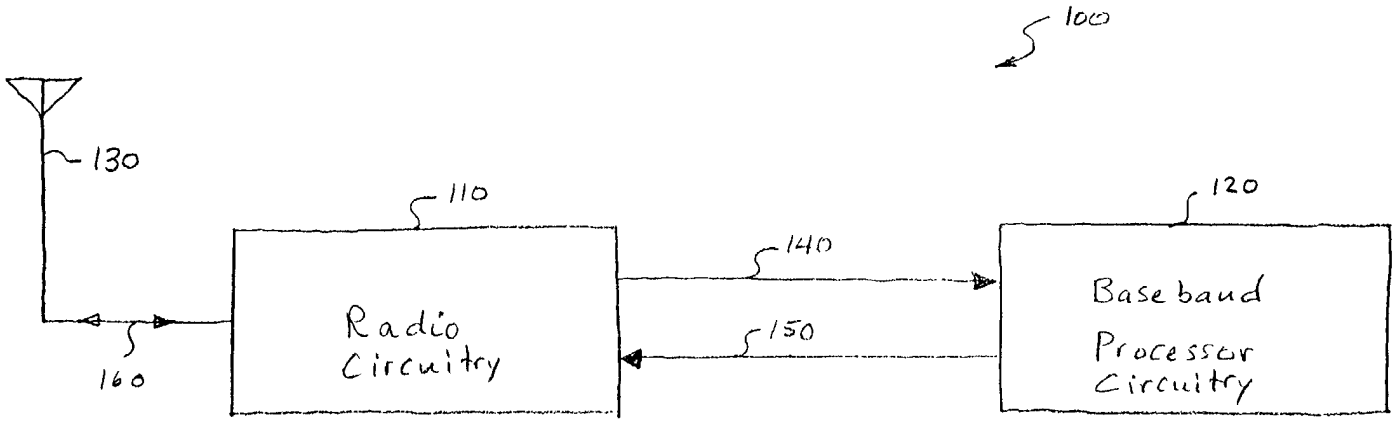


FIG. 1

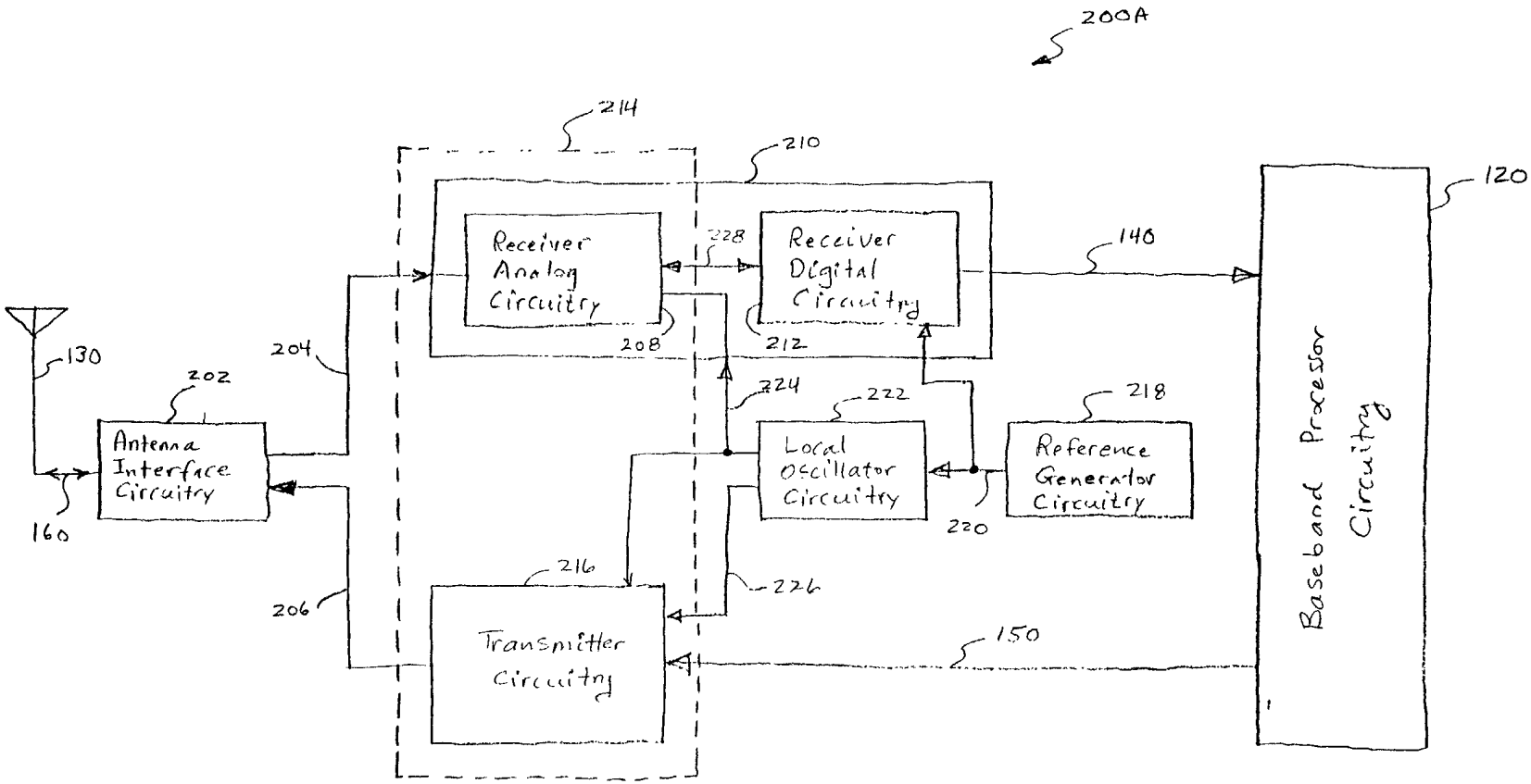

200A
214
210
120
Receiver Analog Circuitry
228
Receiver Digital Circuitry
140
130
202
204
208
212
224
222
218
Antenna Interface Circuitry
Local Oscillator Circuitry
Reference Generator Circuitry
160
220
216
206
226
Transmitter Circuitry
150
Baseband Processor Circuitry

FIG. 2A

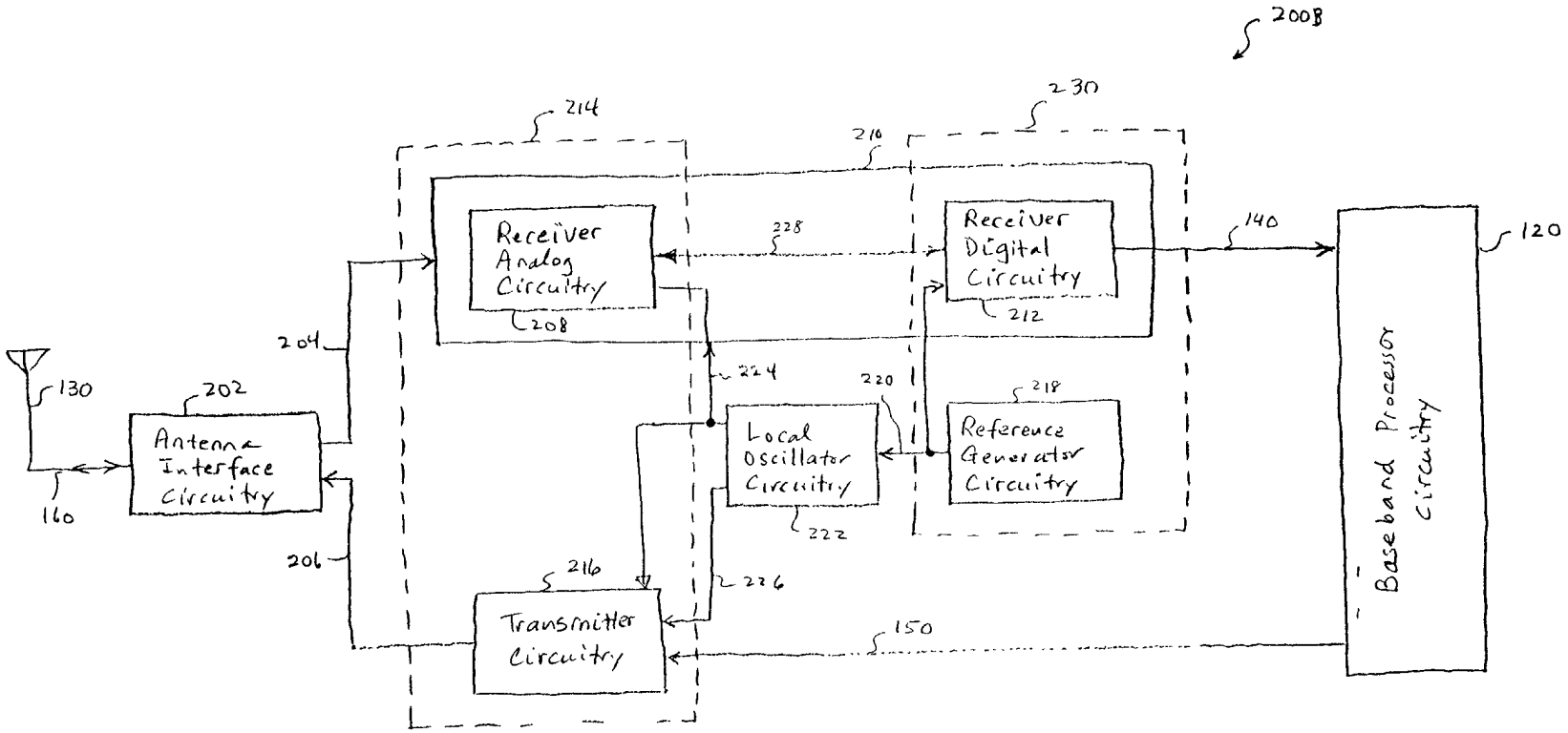

200B
214
230
210
Receiver Analog Circuitry
208
228
Receiver Digital Circuitry
212
140
120
Baseband Processor Circuitry
204
130
202
Antenna Interface Circuitry
160
224
220
218
Local Oscillator Circuitry
222
Reference Generator Circuitry
206
216
226
Transmitter Circuitry
150

FIG. 2B

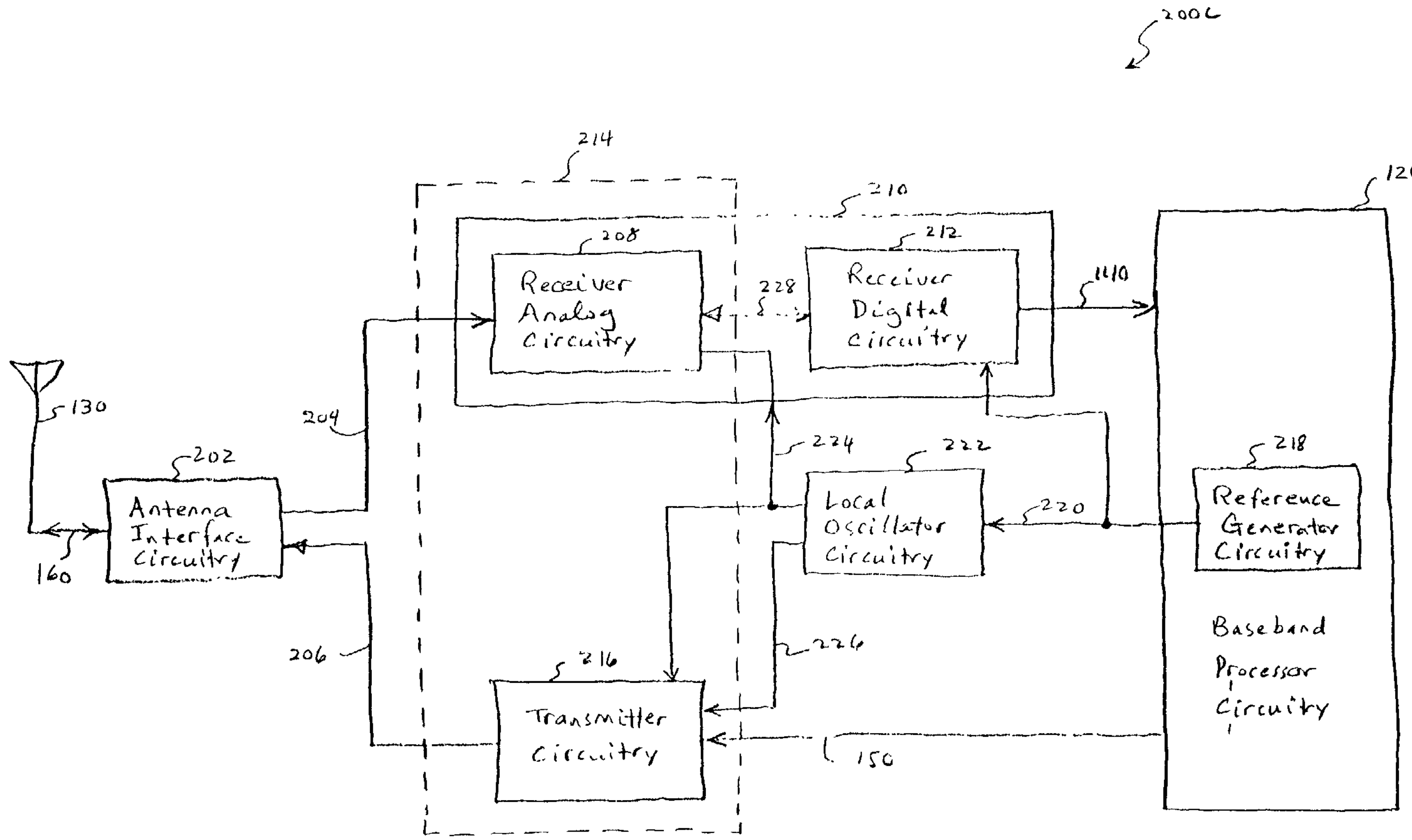

200C
214
210
120
208
Receiver Analog Circuitry
228
212
Receiver Digital Circuitry
140
130
204
202
Antenna Interface Circuitry
160
224
222
Local Oscillator Circuitry
220
218
Reference Generator Circuitry
Baseband Processor Circuitry
206
216
Transmitter Circuitry
226
150

FIG. 2C

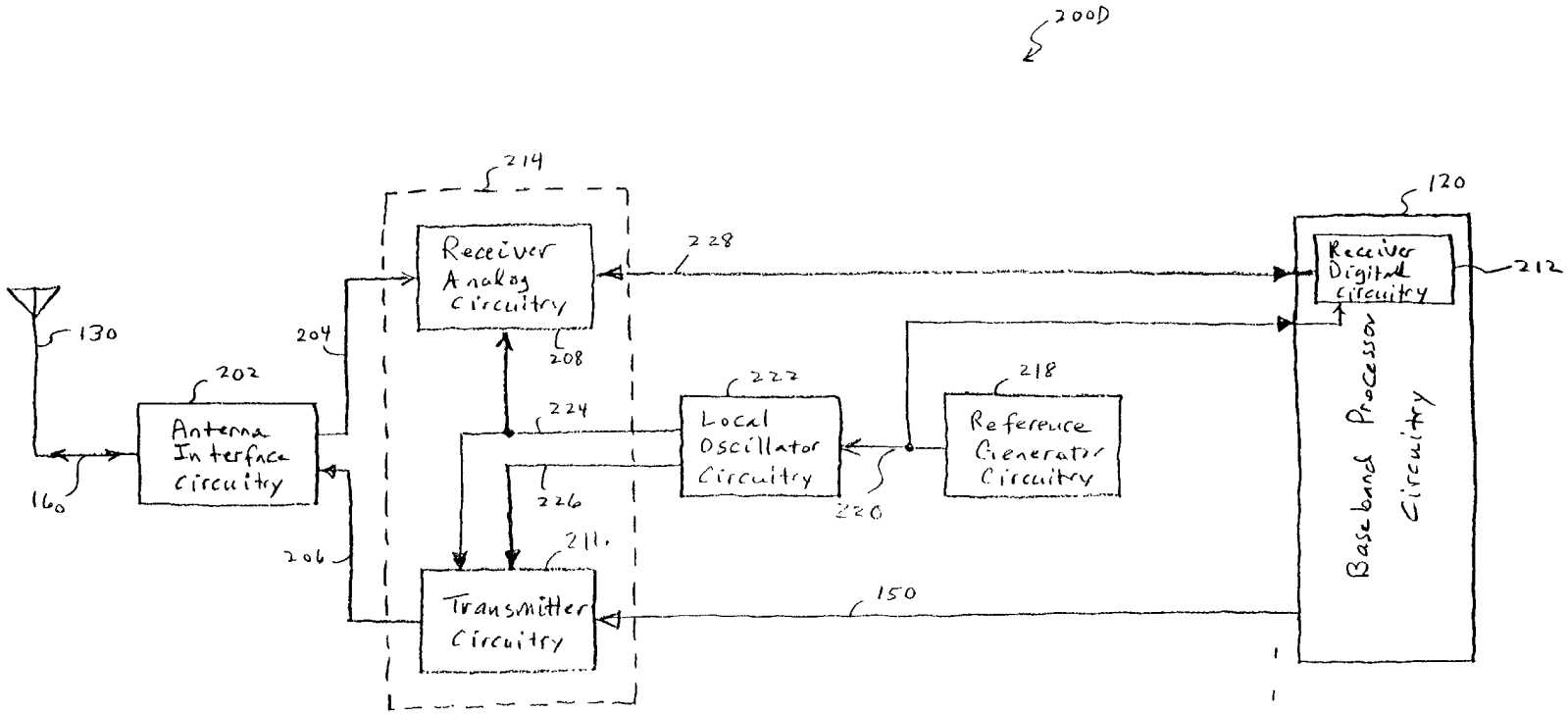

200D
214
120
Receiver Analog Circuitry
228
Receiver Digital Circuitry
212
130
204
208
202
Antenna Interface Circuitry
160
224
222
Local Oscillator Circuitry
218
Reference Generator Circuitry
220
226
211
206
Transmitter Circuitry
150
Baseband Processor Circuitry

FIG. 2D

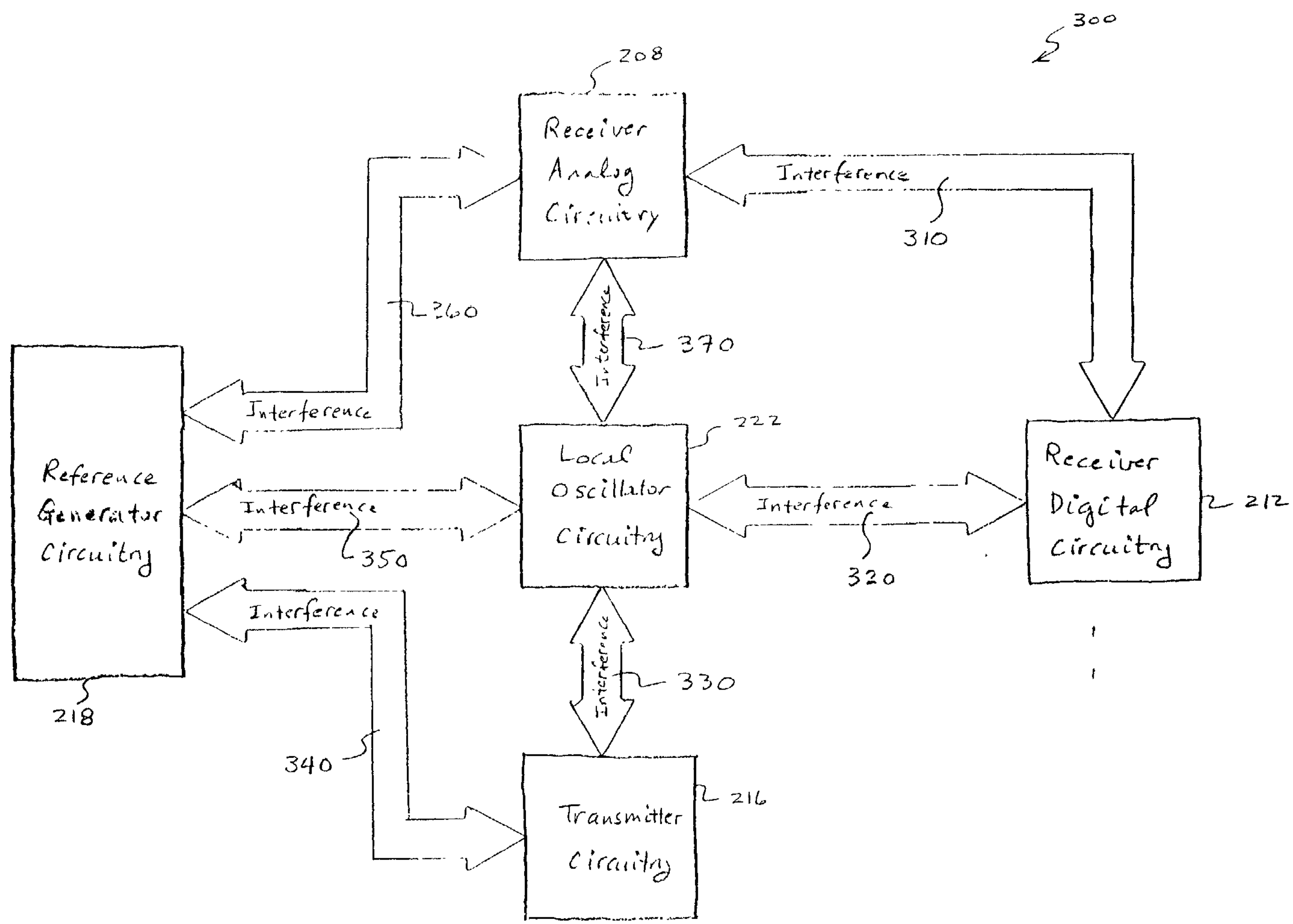

300
208
Receiver Analog Circuitry
Interference
310
260
370
Interference
Reference Generator Circuitry
Interference
350
222
Local Oscillator Circuitry
Interference
320
Receiver Digital Circuitry
212
Interference
218
330
Interference
340
Transmitter Circuitry
216

FIG. 3

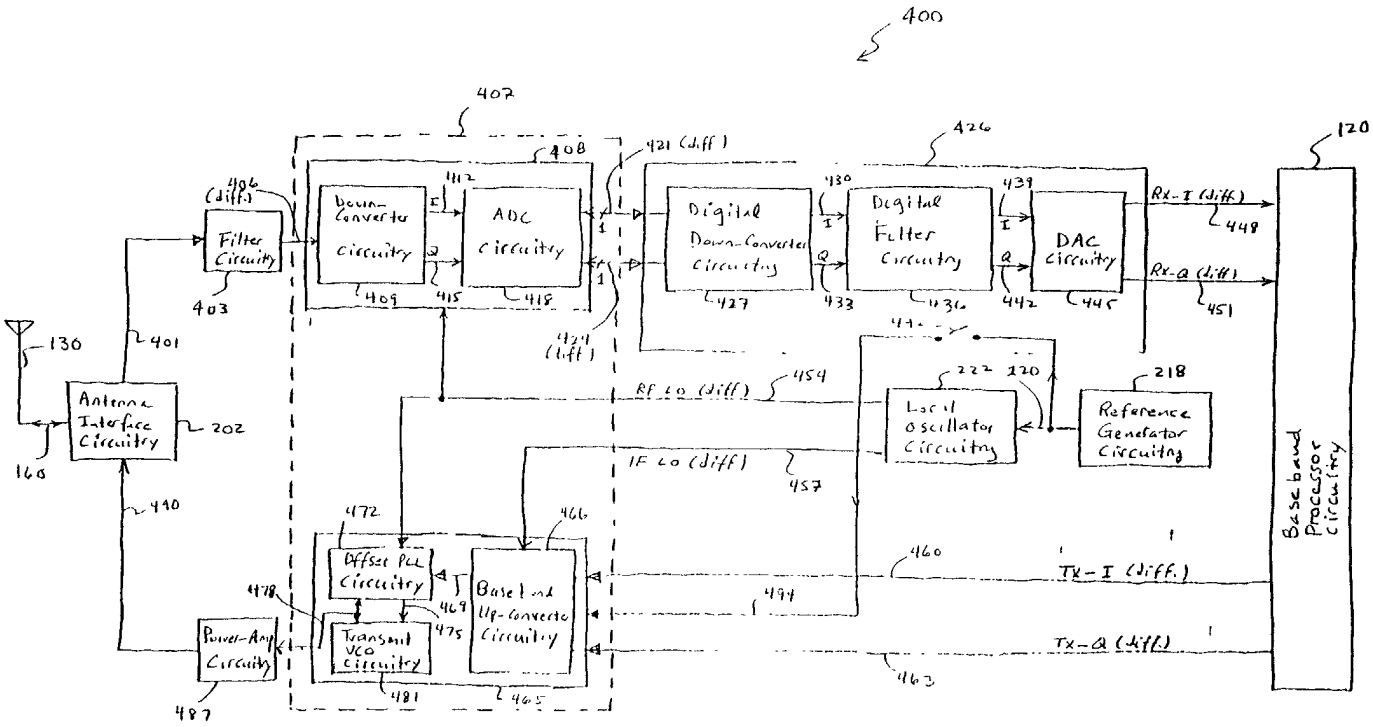

400
407
408
421 (Diff.)
426
120
406 (Diff.)
Filter Circuitry
403
Down-Converter Circuitry
412
I
Q
ADC Circuitry
409
415
418
1
1
424 (Diff.)
Digital Down-Converter Circuitry
427
430
I
Q
433
Digital Filter Circuitry
436
439
I
Q
442
DAC Circuitry
445
Rx-I (Diff.)
448
Rx-Q (Diff.)
451
130
401
Antenna Interface Circuitry
202
160
440
RF LO (Diff.)
454
IF LO (Diff.)
457
222
220
Local Oscillator Circuitry
218
Reference Generator Circuitry
472
466
Offset PLL Circuitry
469
Baseband Up-Converter Circuitry
478
475
Transmit VCO Circuitry
481
465
Power-Amp Circuitry
487
460
Tx-I (Diff.)
494
Tx-Q (Diff.)
463
Baseband Processor Circuitry

FIG. 4

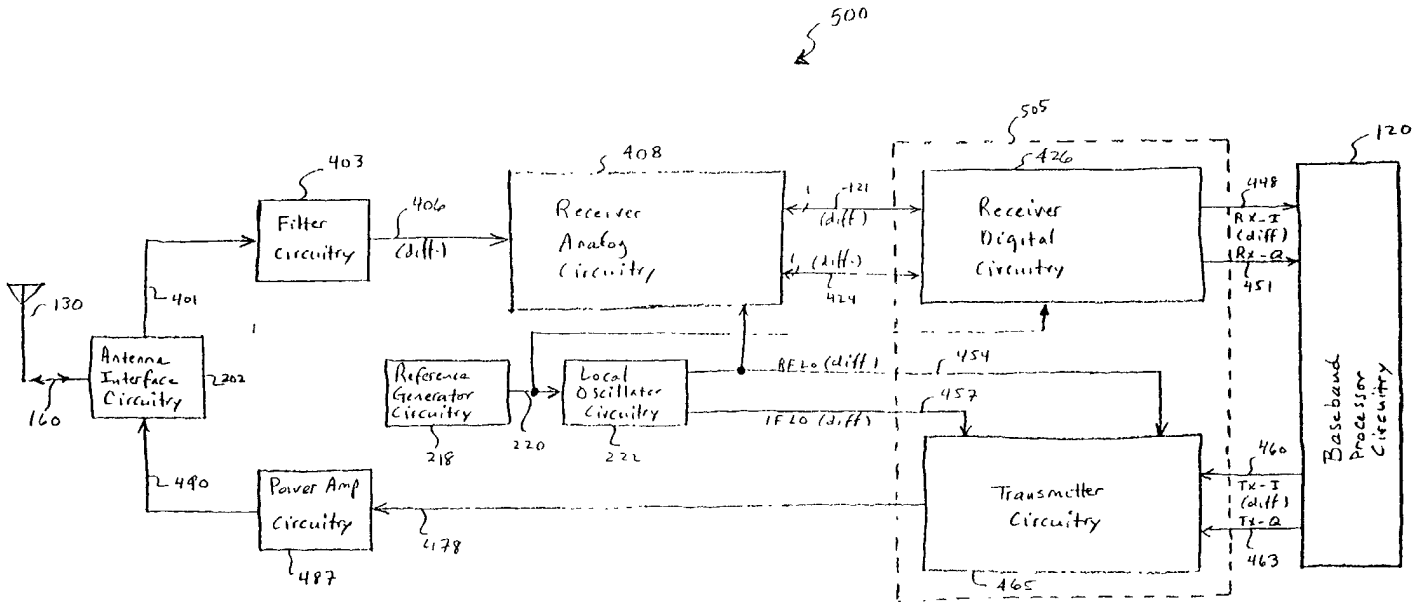

500
505
120
403
408
426
406
(diff.)
Filter Circuitry
Receiver Analog Circuitry
Receiver Digital Circuitry
121
(diff.)
I (diff.)
424
448
RX-I (diff.)
RX-Q
451
130
401
Antenna Interface Circuitry
202
160
Reference Generator Circuitry
218
220
Local Oscillator Circuitry
222
RF LO (diff.)
454
IF LO (diff.)
457
Baseband Processor Circuitry
460
TX-I (diff.)
TX-Q
463
Transmitter Circuitry
465
490
Power Amp Circuitry
478
487

FIG. 5

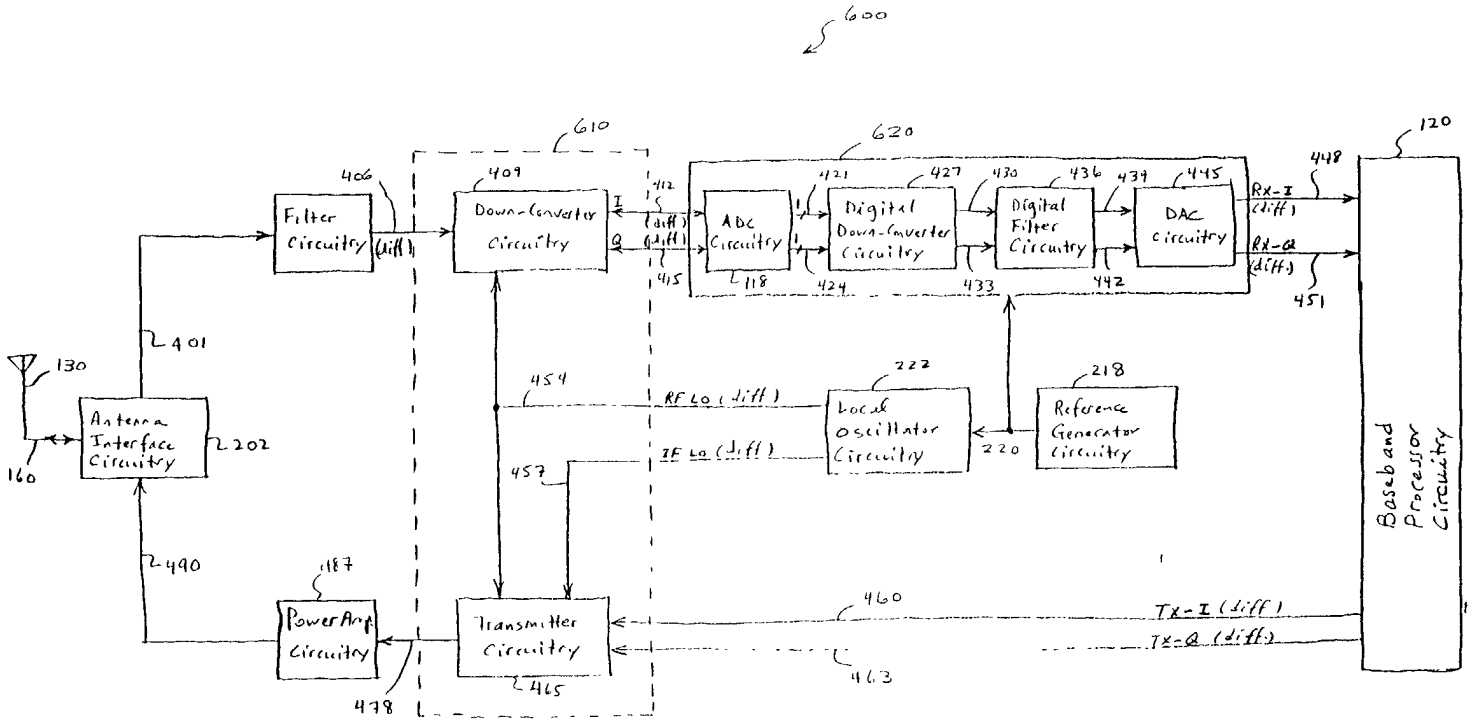


FIG. 6

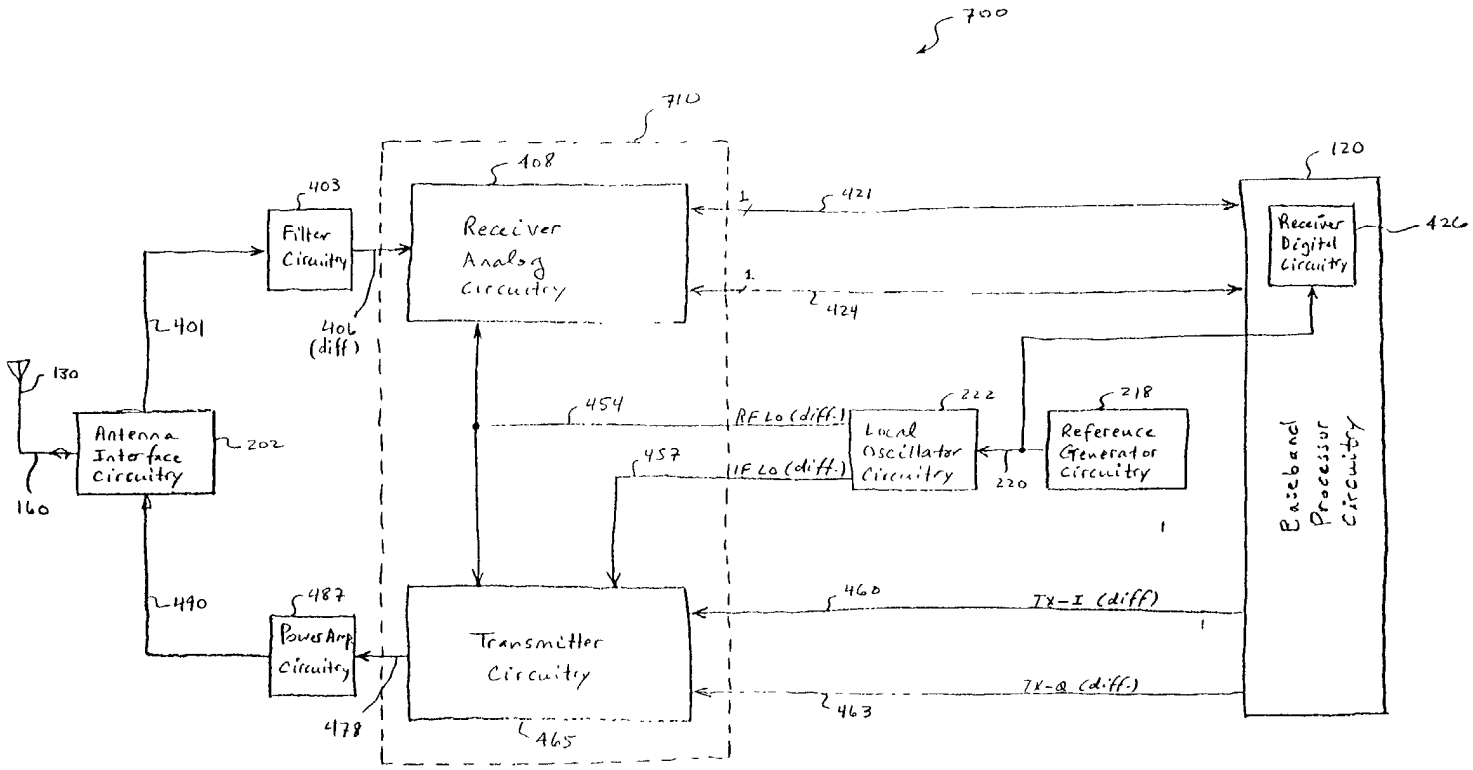


FIG. 7

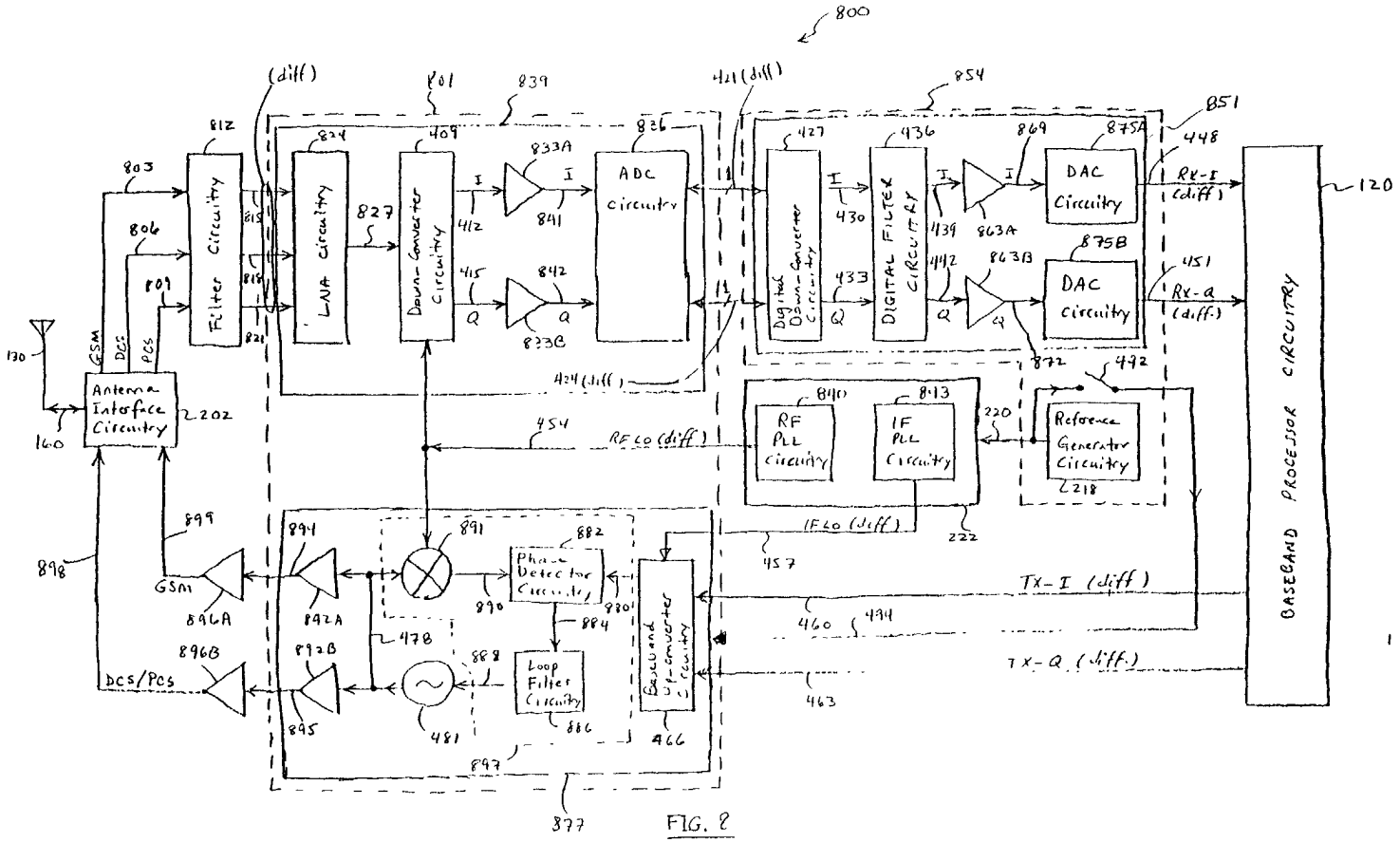

800
(diff)
801
839
421 (diff)
854
851
812
824
809
826
427
436
869
875A
448
803
806
809
827
833A
841
ADC circuitry
Digital Down-Converter Circuitry
DIGITAL FILTER CIRCUITRY
DAC Circuitry
Rx-I (diff)
120
Filter Circuitry
LNA circuitry
Down-Converter Circuitry
412
430
439
863A
875B
451
Rx-Q (diff)
130
GSM
DCS
PCS
815
818
821
415
842
833B
433
442
863B
872
472
424 (diff)
Antenna Interface Circuitry
202
160
454
RF LO (diff)
840
843
220
RF PLL circuitry
IF PLL Circuitry
Reference Generator Circuitry
218
222
IF LO (diff)
457
899
894
891
882
898
Phase Detector Circuitry
Tx-I (diff)
GSM
896A
892A
890
880
884
460
494
478
888
896B
892B
Tx-Q (diff)
DCS/PCS
Loop Filter Circuitry
Baseband Up-converter Circuitry
463
481
886
466
895
897
877
BASEBAND PROCESSOR CIRCUITRY

FIG. 8

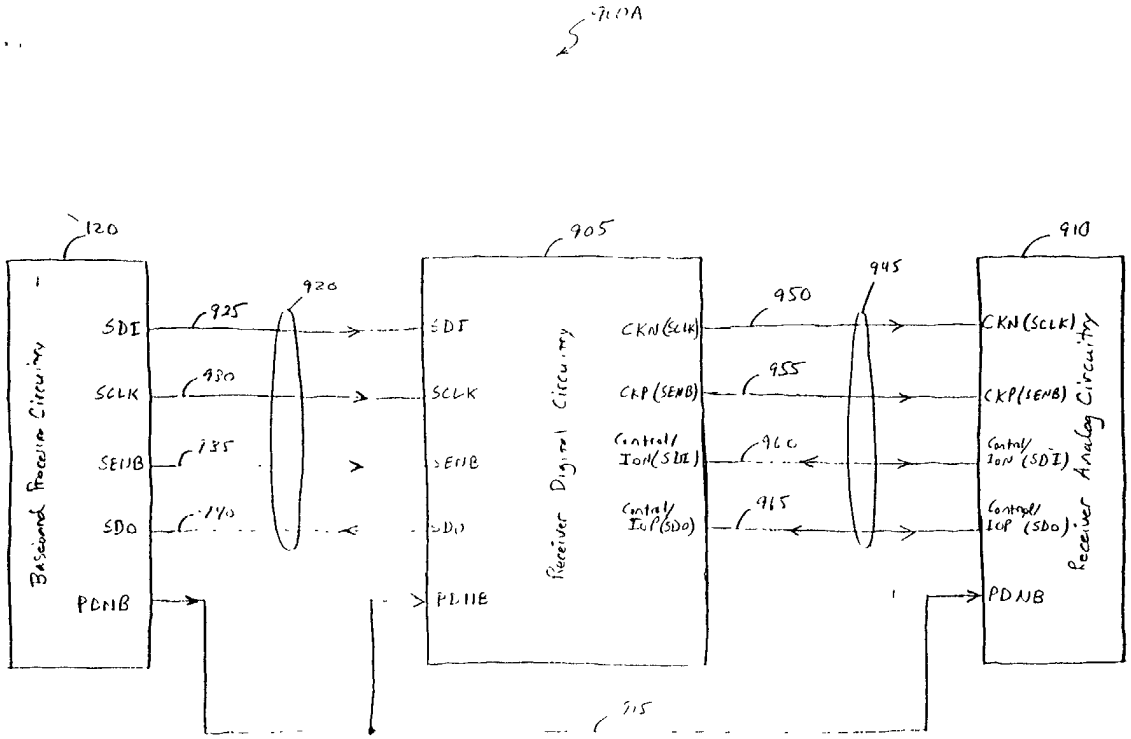


FIG. 9A

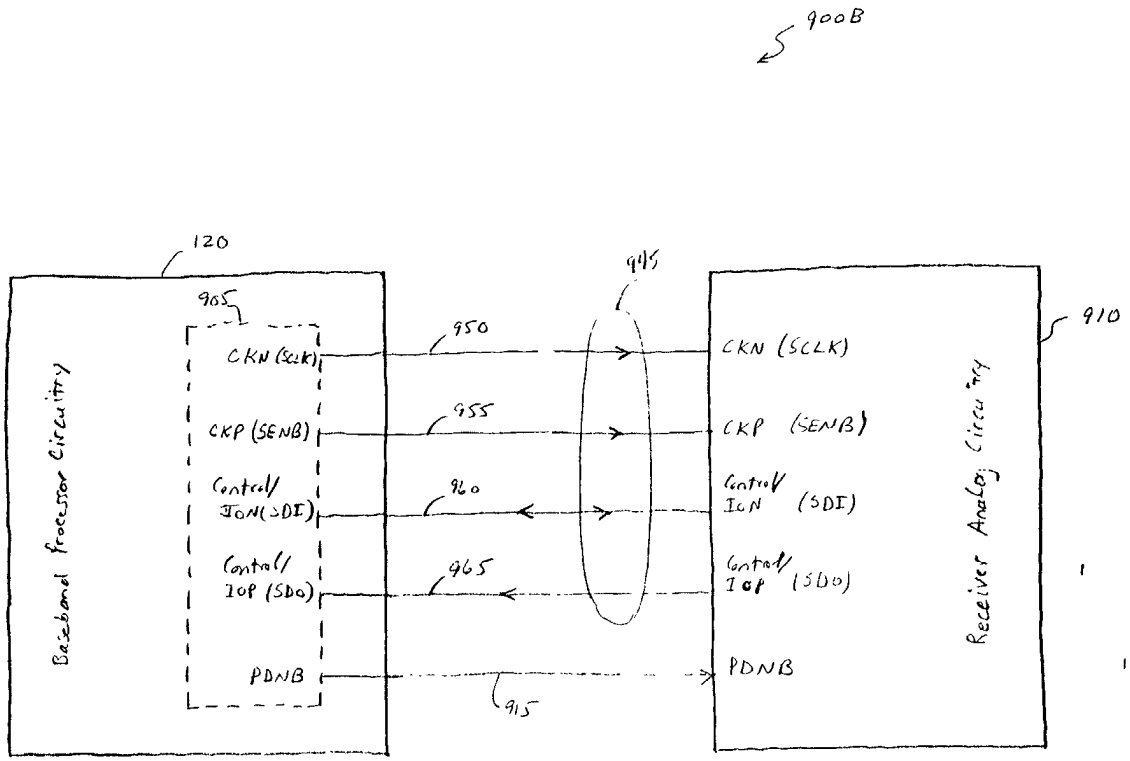

900B
120
905
Baseband Processor Circuitry
CKN (SCLK)
CKP (SENB)
Control IOP (SDO)
PDNB
950
955
960
965
915
945
CKN (SCLK)
CKP (SENB)
Control IOP (SDO)
PDNB
910
Receiver Analog Circuitry

FIG. 9B

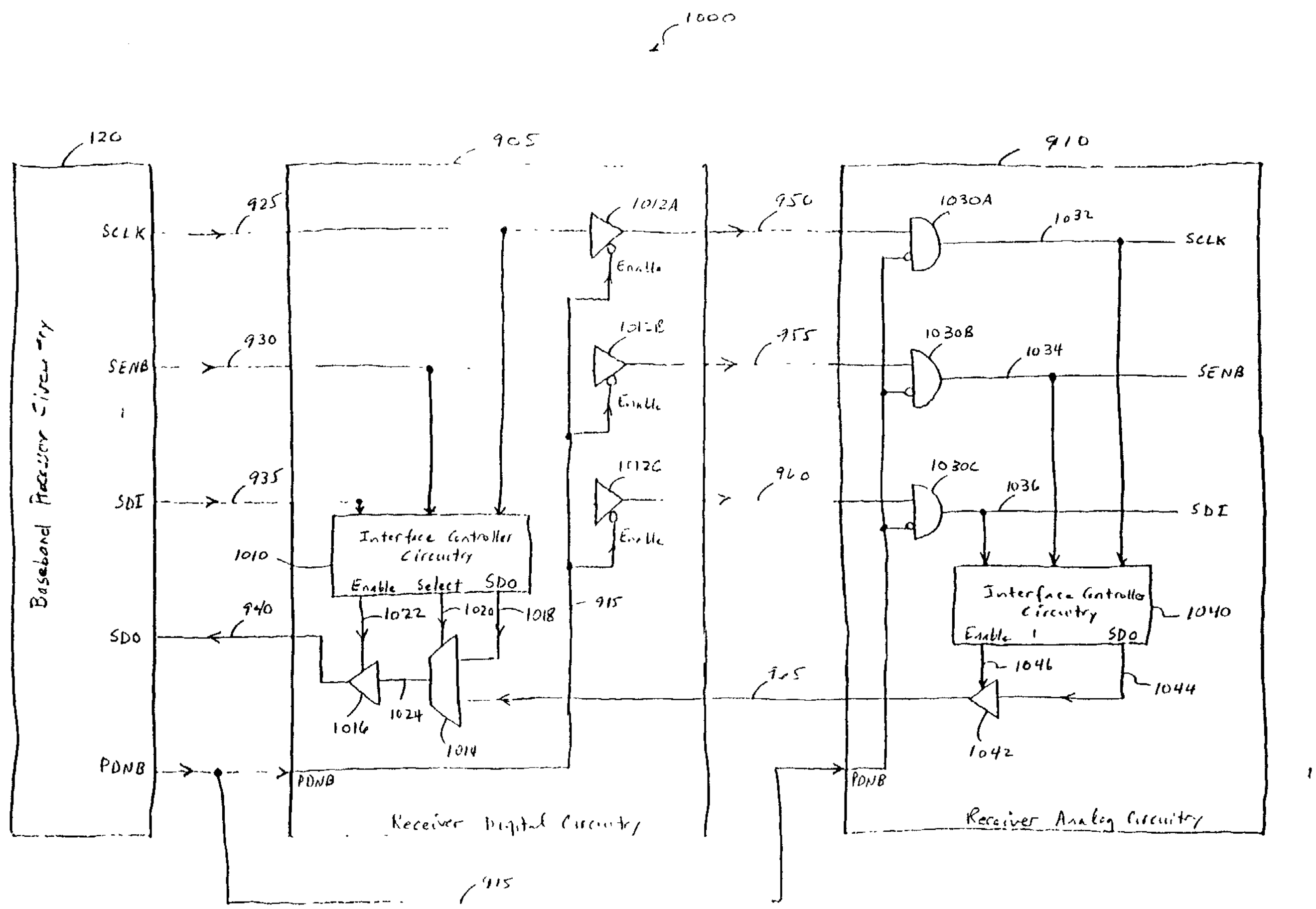
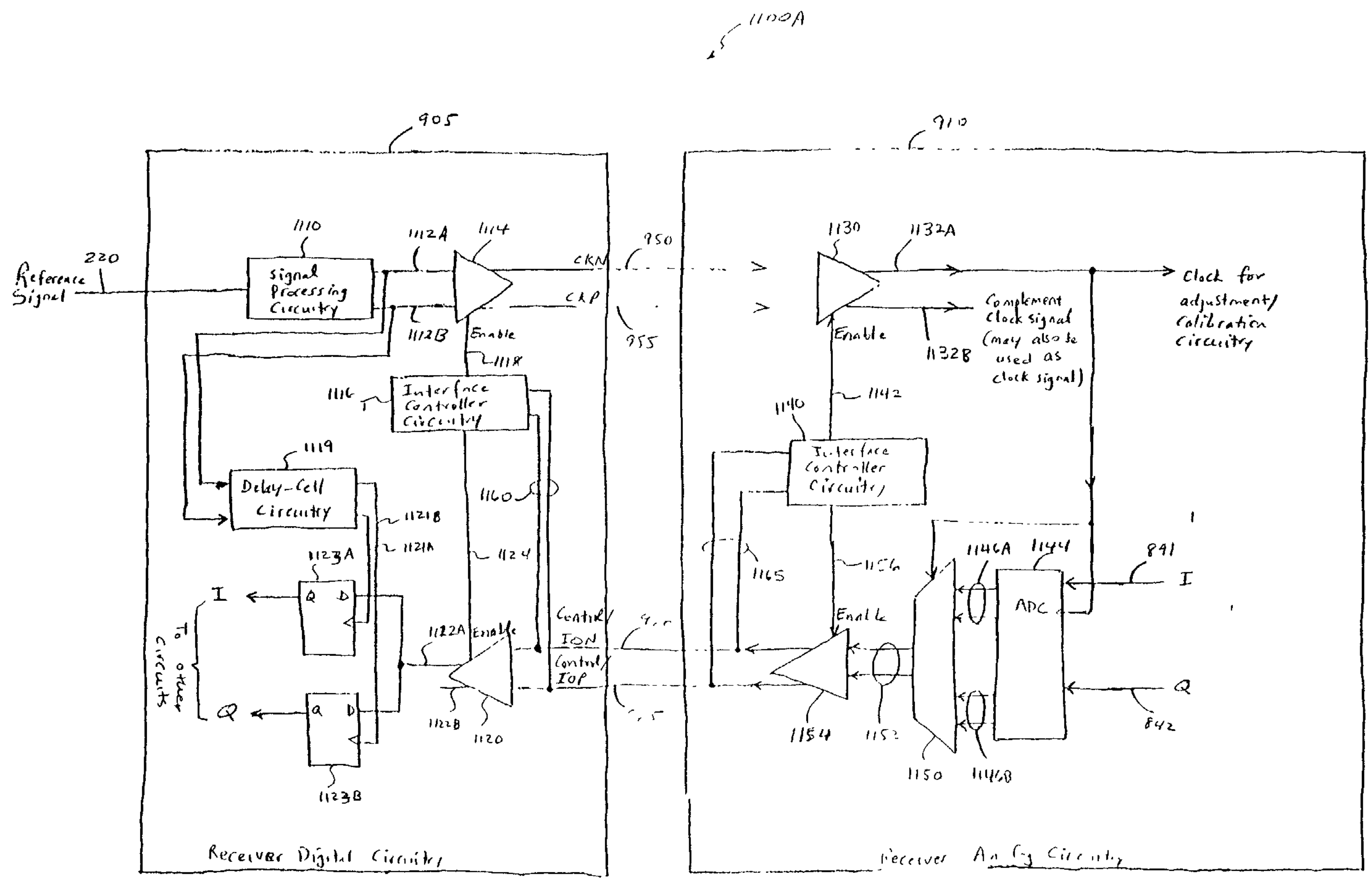

1000
120
905
910
Baseband Receiver Circuitry
SCLK
SENB
SDI
SDO
PDNB
925
930
935
940
950
955
960
915
Interface Controller Circuitry
Enable Select SDO
1010
1012A
1012B
1012C
1014
1016
1018
1020
1022
1024
Receiver Digital Circuitry
1030A
1030B
1030C
1032
1034
1036
1040
1042
1044
1046
Receiver Analog Circuitry

FIG. 10



1100A
905
910
Reference Signal
220
Signal Processing Circuitry
1110
1112A
1114
1112B
CKN
CKP
950
955
Enable
1118
Interface Controller Circuitry
1116
1119
Delay-Cell Circuitry
1121B
1121A
1160
1124
1123A
1123B
I
Q
To other circuits
1122A
Enable
1122B
1120
Control ION
Control IOP
1130
1132A
Enable
1132B
Complement Clock signal (may also be used as clock signal)
Clock for adjustment/calibration circuitry
1142
1140
Interface Controller Circuitry
1165
1156
Enable
1154
1152
1150
1146A
1146B
1144
ADC
841
842
Receiver Digital Circuitry

FIG. 11A

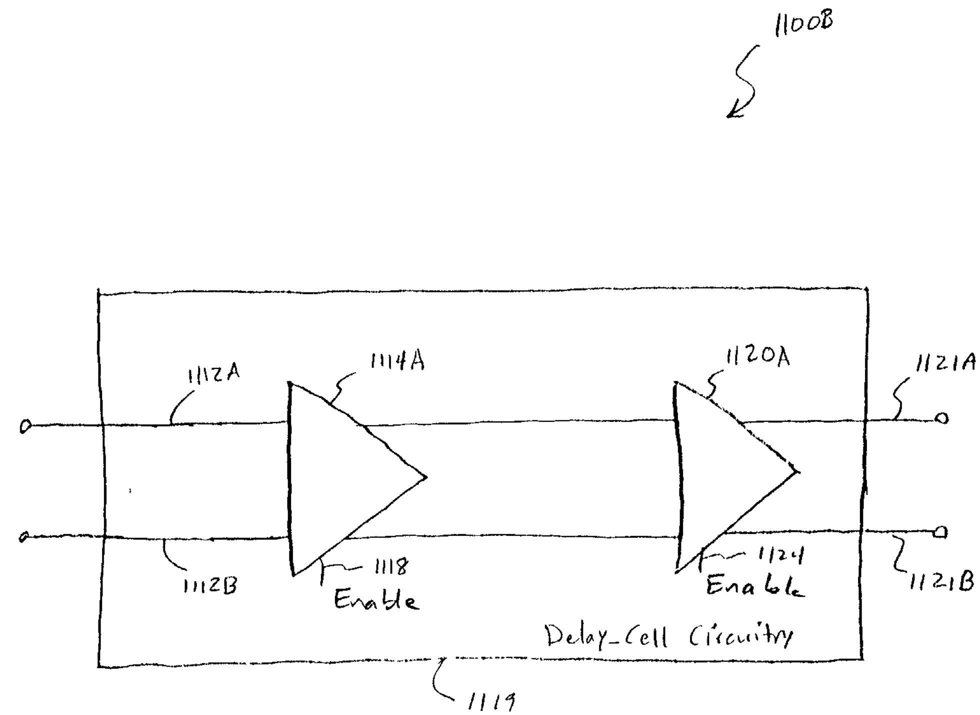

1100B
1112A
1114A
1120A
1121A
1112B
1118
Enable
1124
Enable
1121B
Delay_Cell Circuitry
1119

FIG. 11B

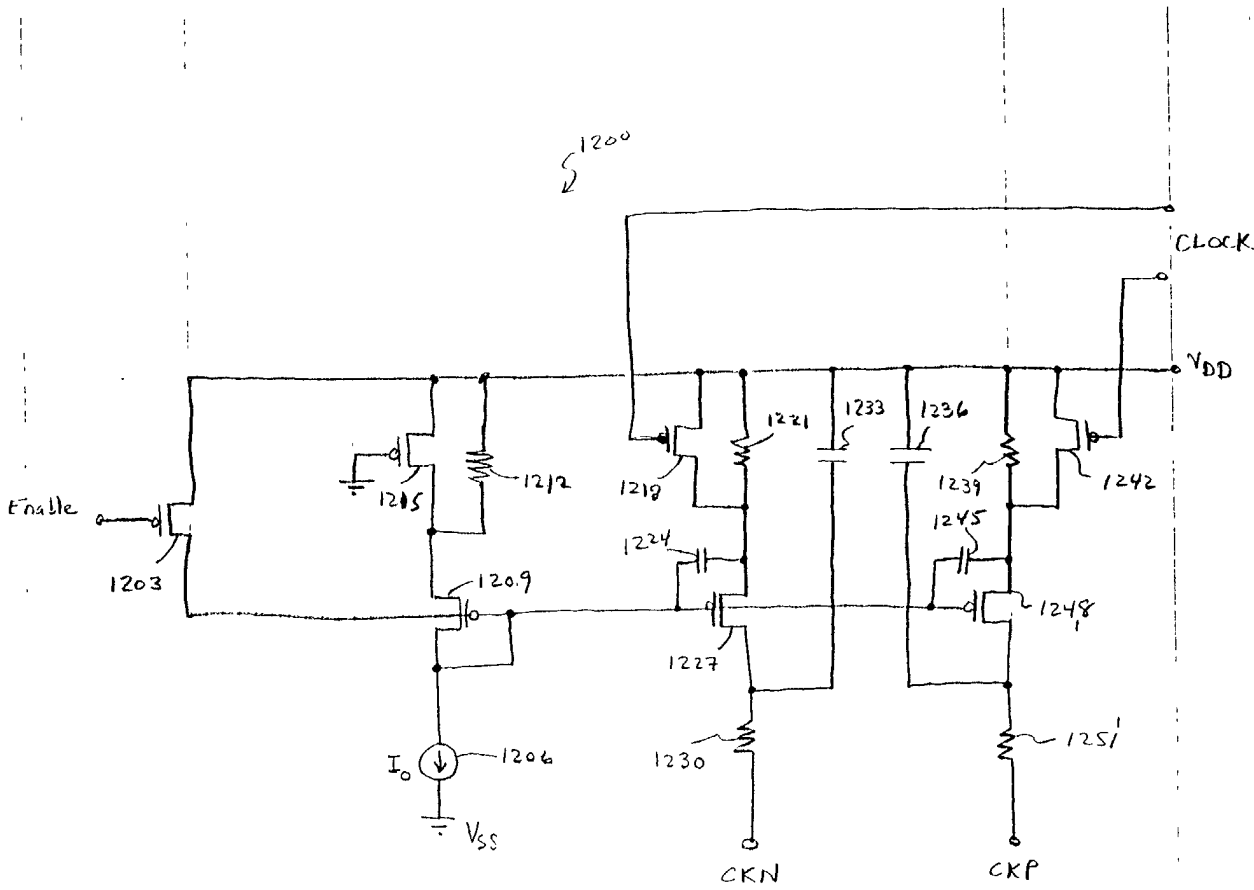


FIG. 12

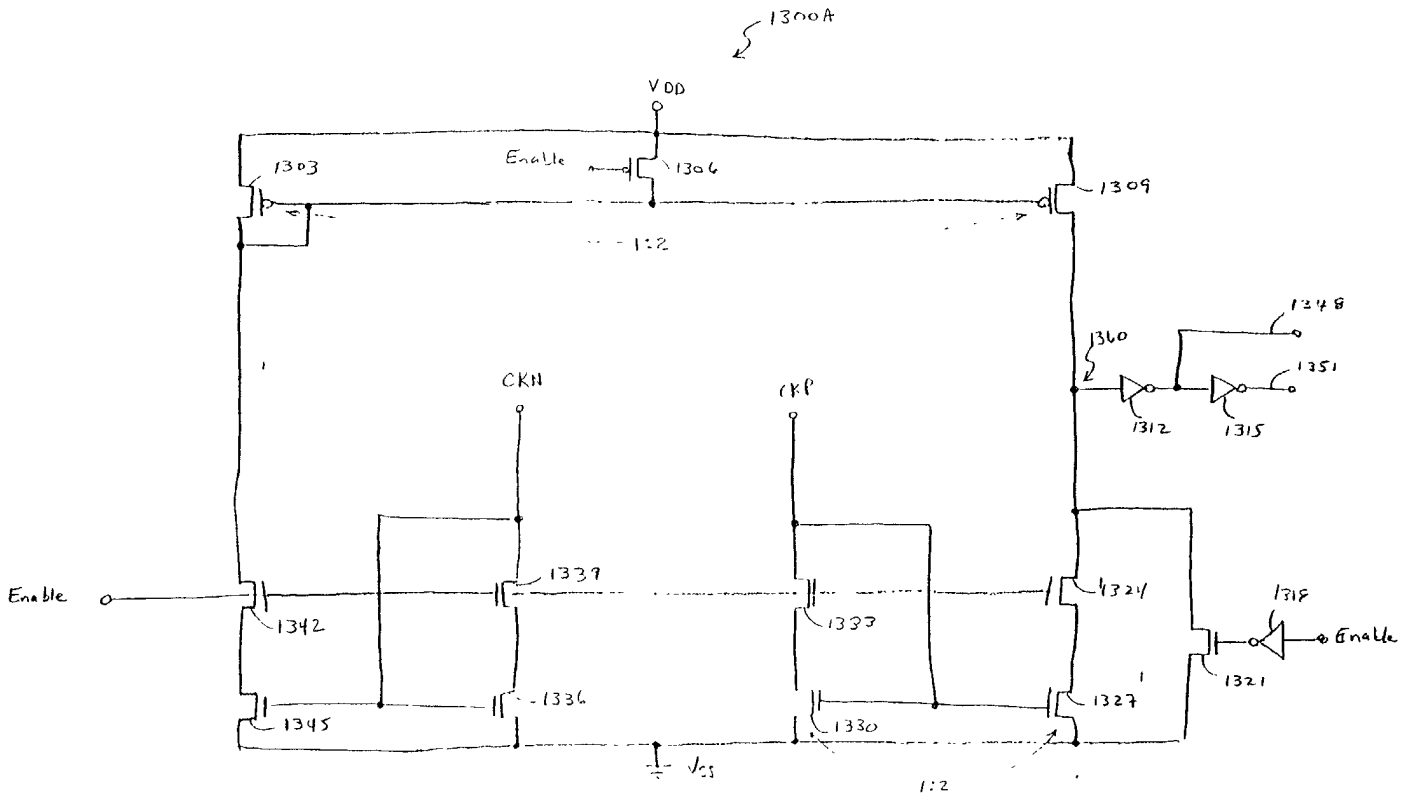


FIG. 13A

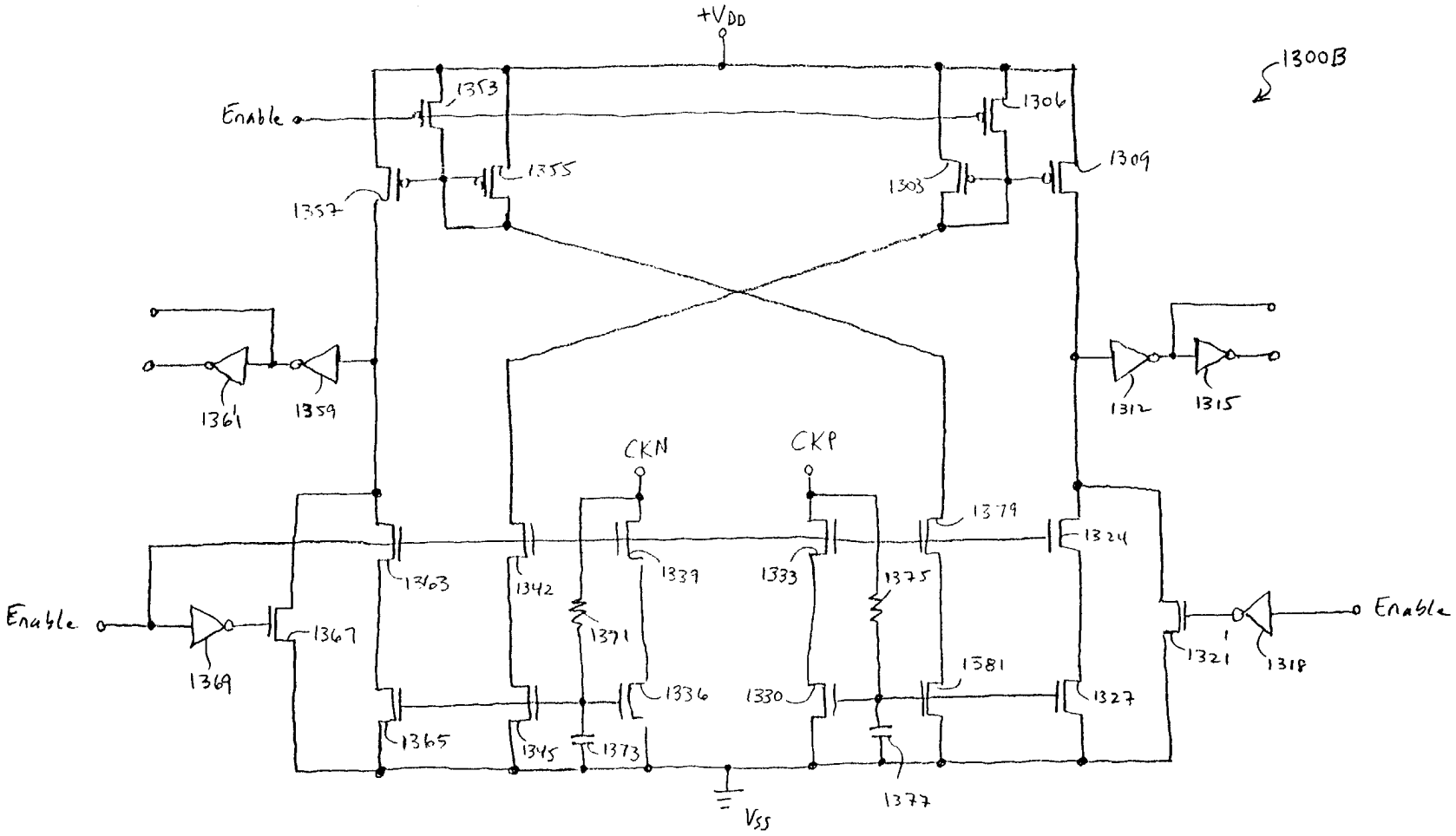

+VDD
1300B
Enable
1353
1306
1355
1309
1357
1303
1361
1359
1312
1315
CKN
CKP
1379
1324
1363
1342
1339
1333
1375
Enable
1367
1371
Enable
1369
1321
1318
1381
1336
1330
1327
1365
1345
1373
1377
Vss

FIG. 13B

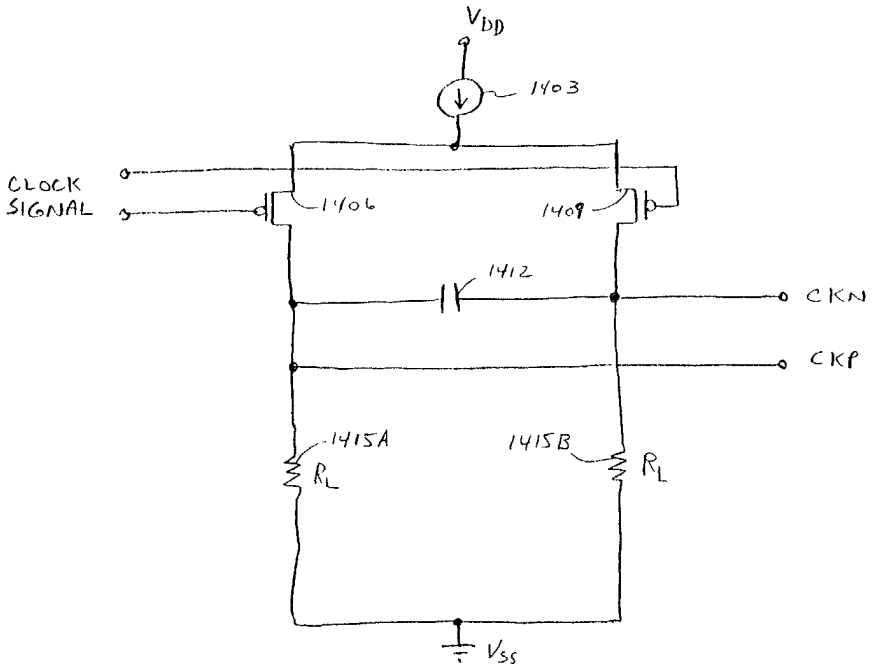

V_{DD}
1403
CLOCK SIGNAL
1406
1409
1412
CKN
CKP
1415A
R_L
1415B
R_L
V_{SS}

FIG. 14

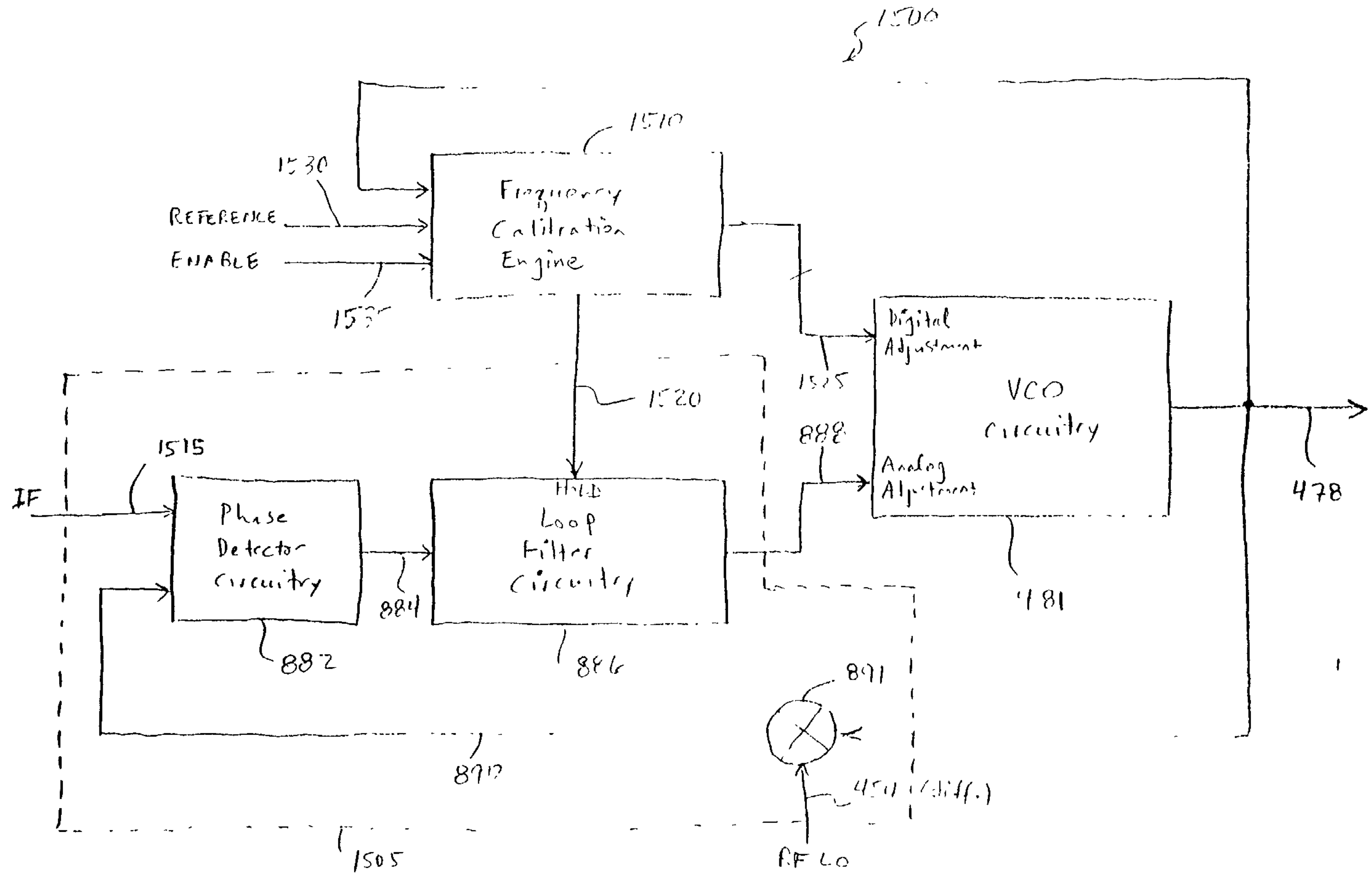

1500
1510
1530
REFERENCE
ENABLE
Frequency
Calibration
Engine
Digital
Adjustment
VCO
circuitry
Analog
Adjustment
1525
888
1520
1515
IF
Phase
Detector
circuitry
HOLD
Loop
Filter
Circuitry
884
882
886
481
478
891
1505
RF LO

FIG. 15

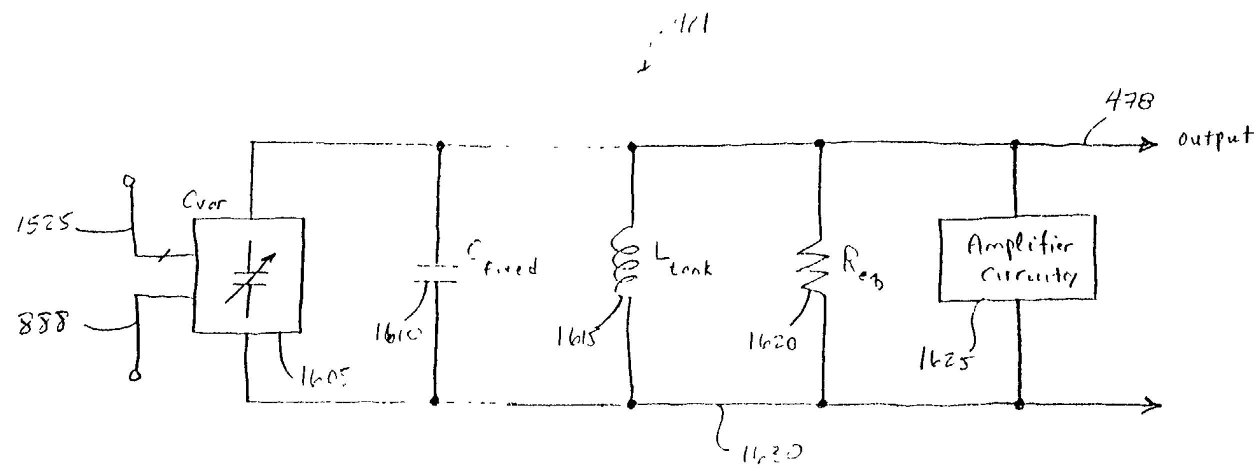

411
478
output
1525
888
Cvar
1605
C fixed
1610
L tank
1615
R eq
1620
Amplifier Circuitry
1625
1630

FIG. 16

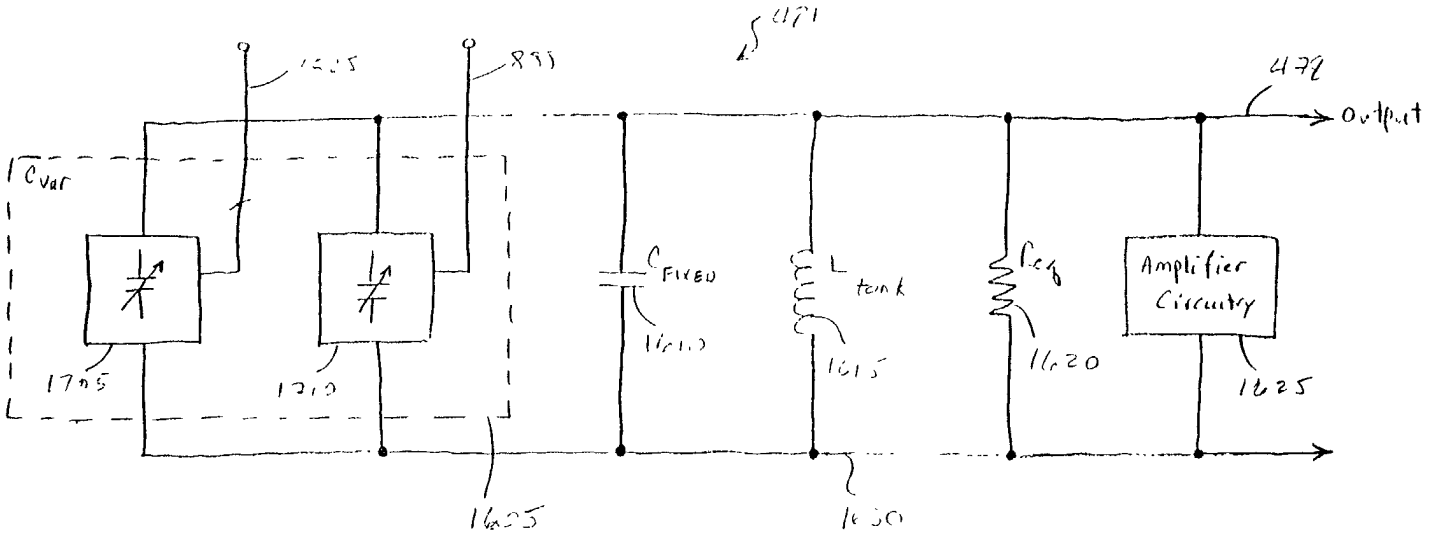


FIG. 17

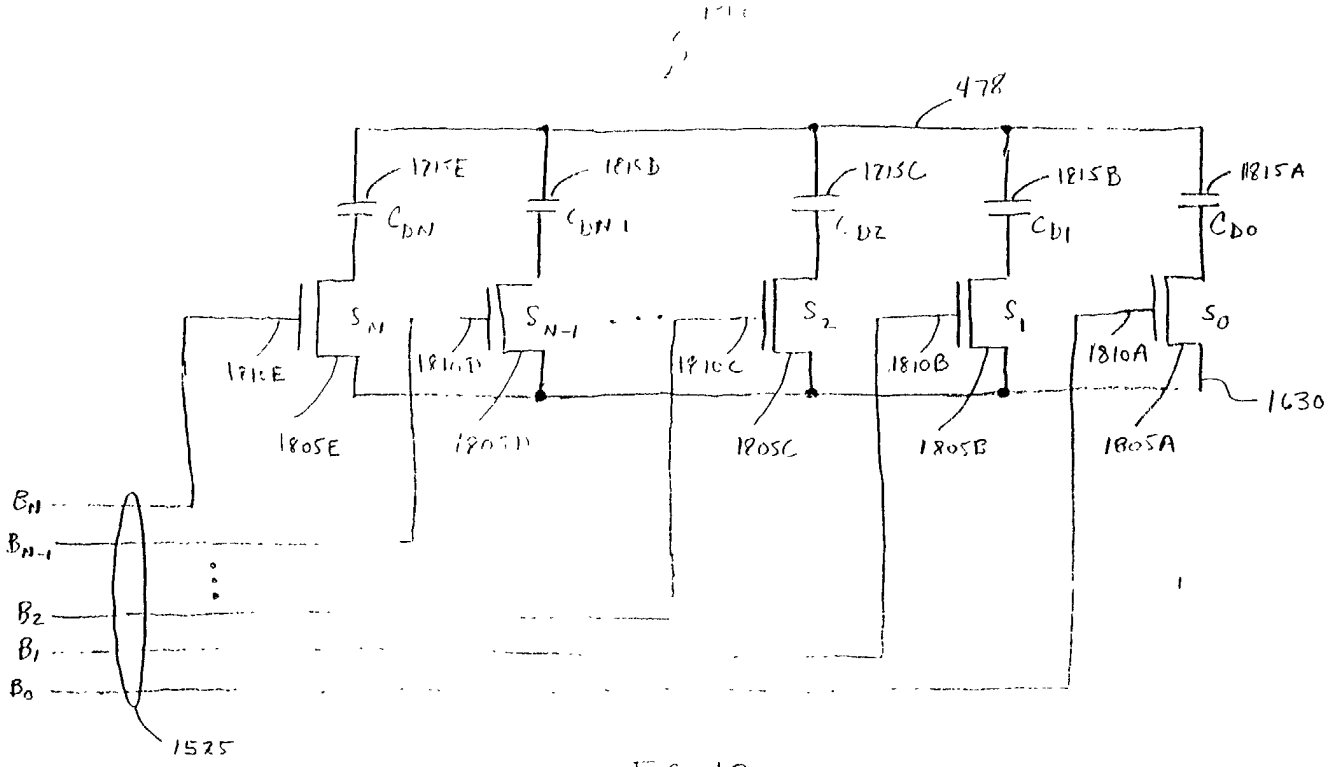

478
1715E
1715D
1715C
1715B
1715A
C_{DN}
C_{DN-1}
C_{D2}
C_{D1}
C_{D0}
S_N
S_{N-1}
S_2
S_1
S_0
1710E
1710D
1710C
1810B
1810A
1805E
1805D
1805C
1805B
1805A
1630
B_N
B_{N-1}
B_2
B_1
B_0
1525

FIG. 18

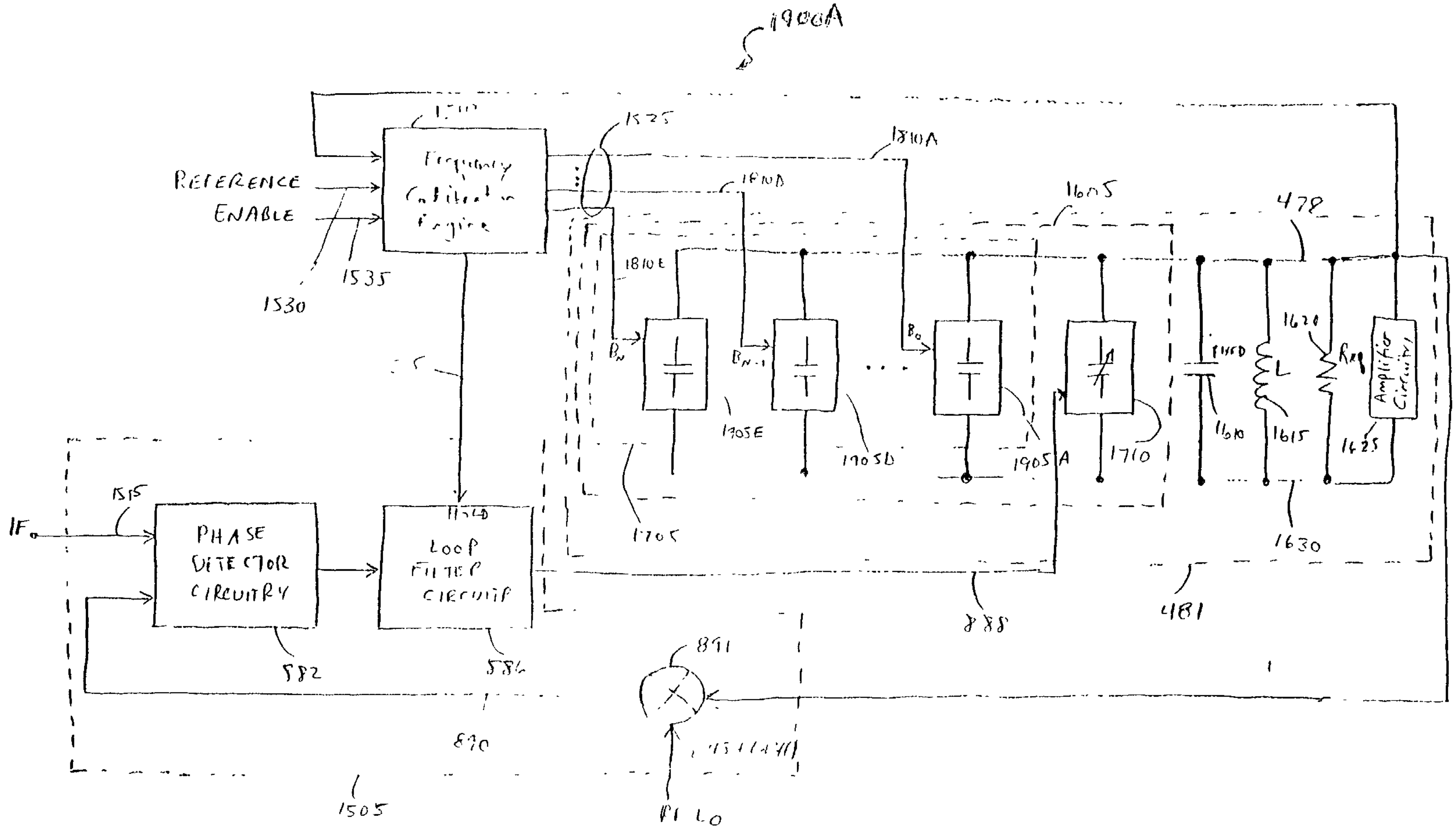

1900A
REFERENCE
ENABLE
1530
1535
Frequency Calibration Engine
1525
1810A
1810D
1810E
1605
478
B_N
B_{N-1}
B_0
1905E
1905D
1905A
1710
FIXED
L
Req
Amplifier Circuitry
1610
1615
1620
1625
1630
1705
IF_0
1515
PHASE DETECTOR CIRCUITRY
LOOP FILTER CIRCUITRY
582
586
888
481
891
890
1505
RF LO

FIG. 19A

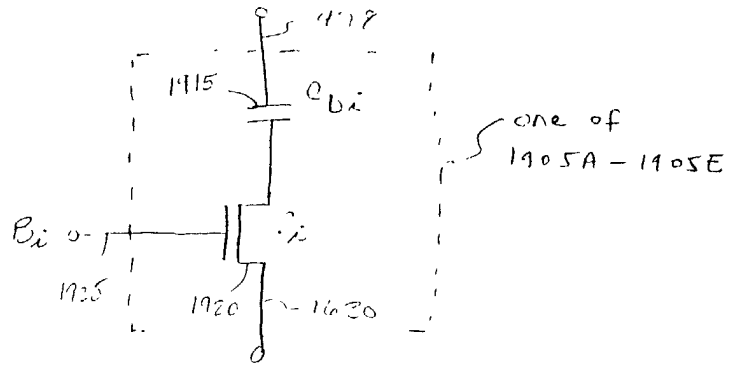


FIG. 19B

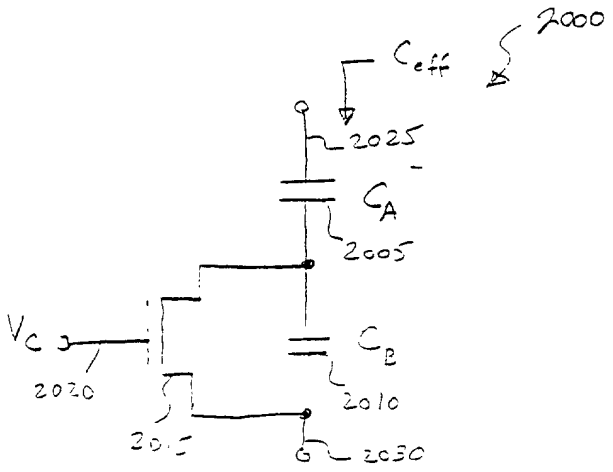

2000
C_{eff}
2025
C_A
2005
V_C
2020
C_B
2010
2015
G
2030

FIG. 20

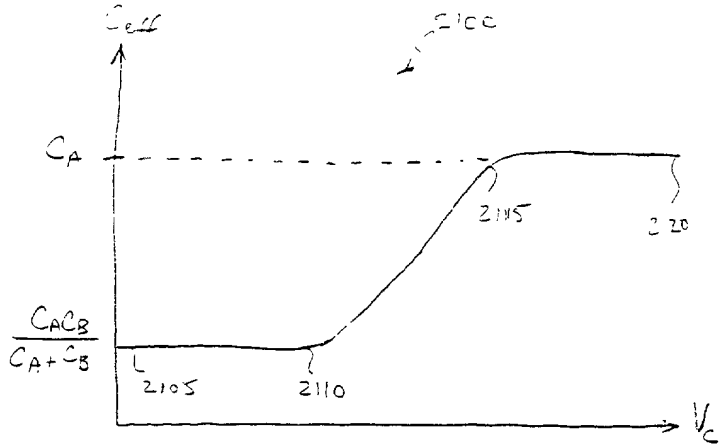

C_{eff}
2100
C_A
2115
2120
$\frac{C_A C_B}{C_A + C_B}$
2105
2110
V_C

FIG. 21

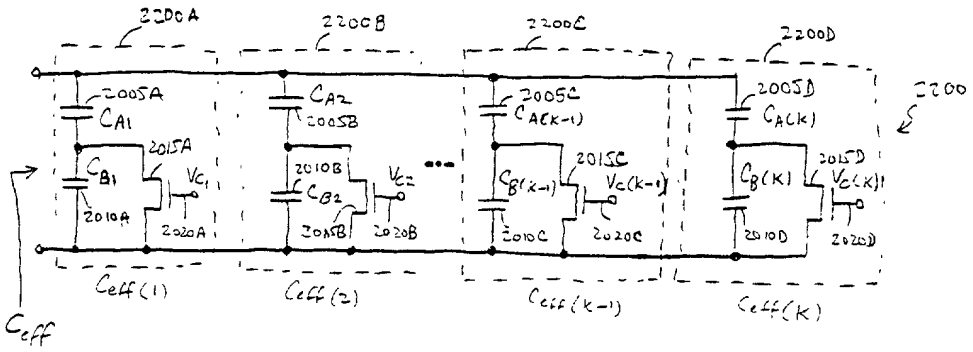


FIG. 22

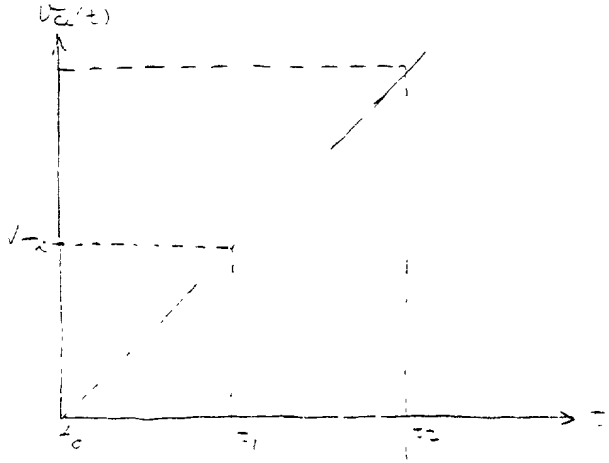


FIG. 23A

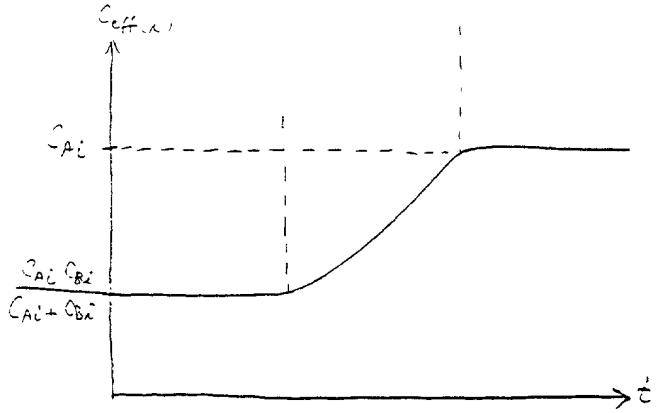


FIG. 23B

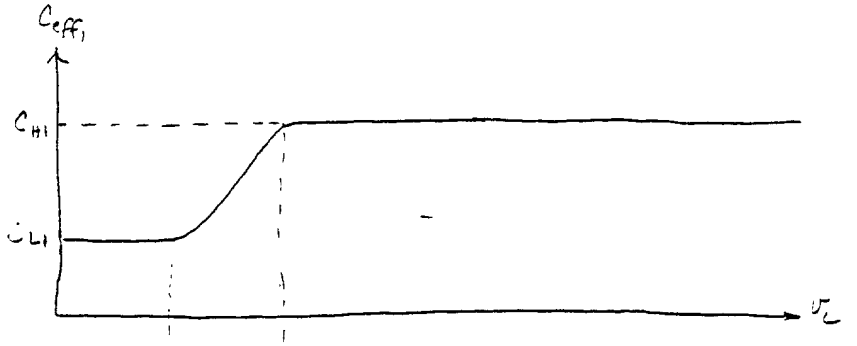


FIG. 24A

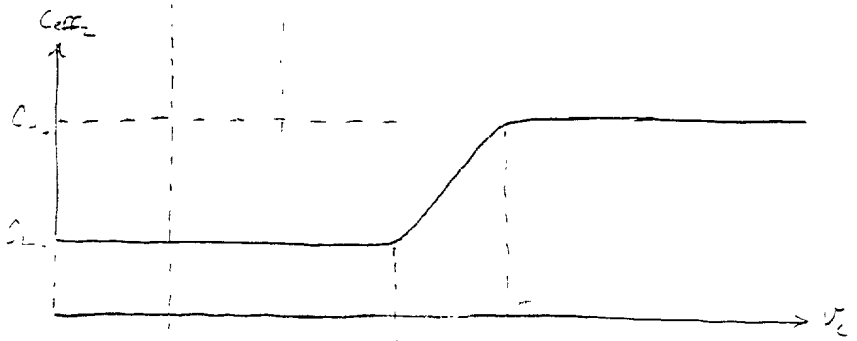


FIG. 24B

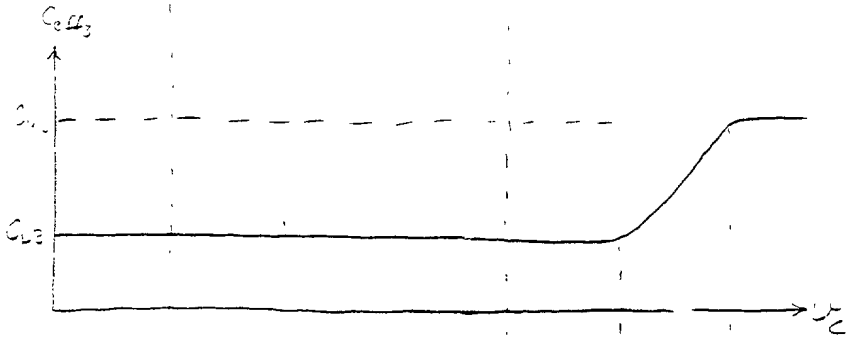


FIG. 24C

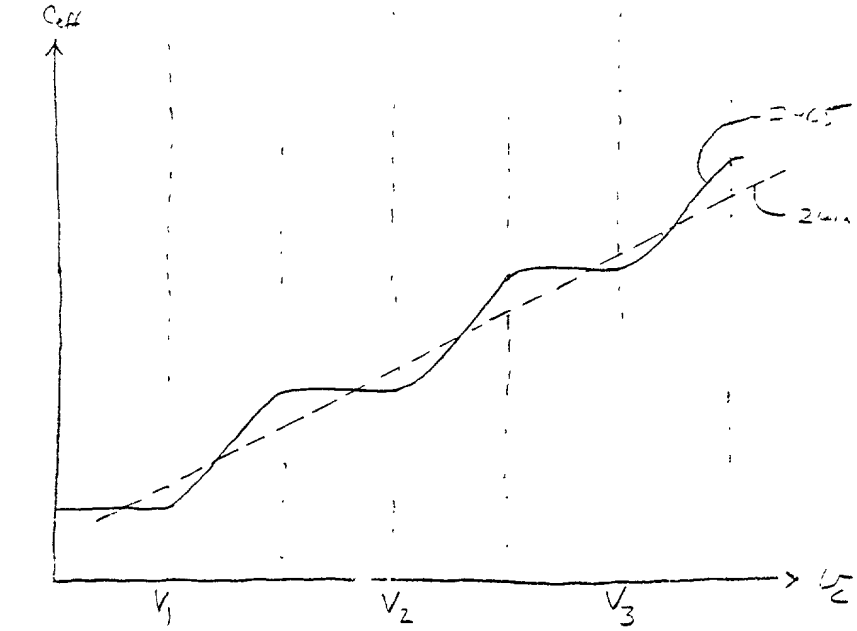


FIG. 24D

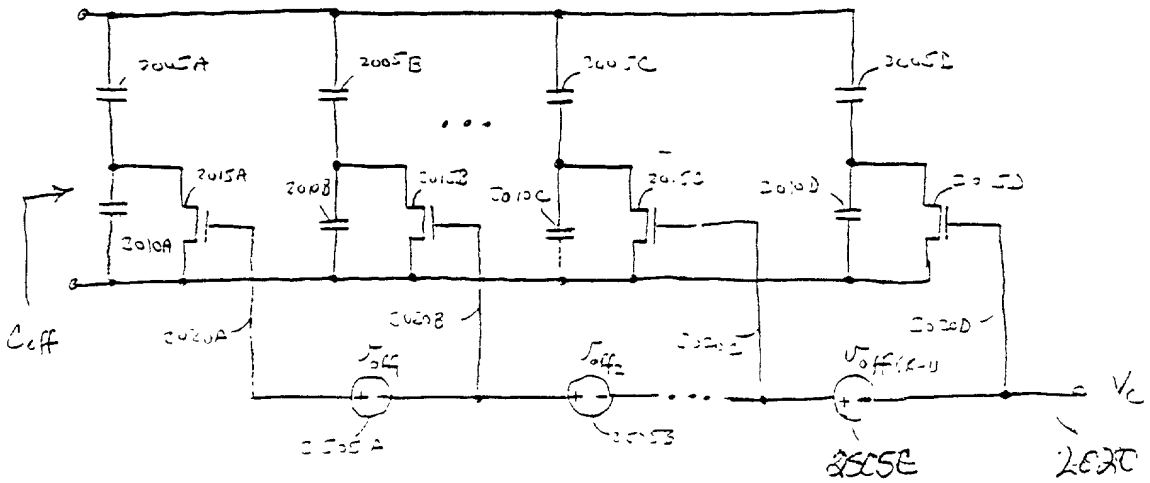


FIG. 25

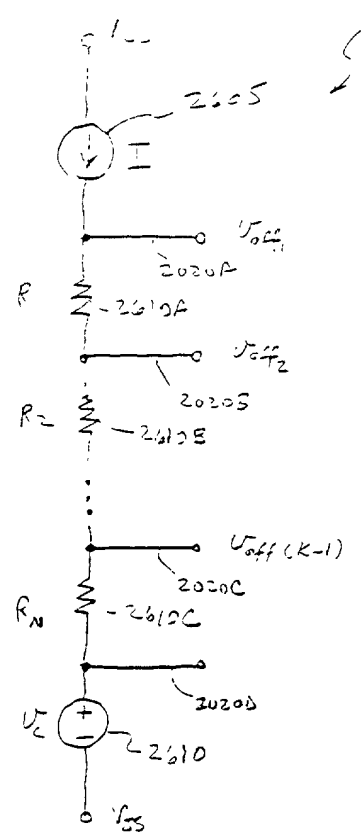


FIG. 26

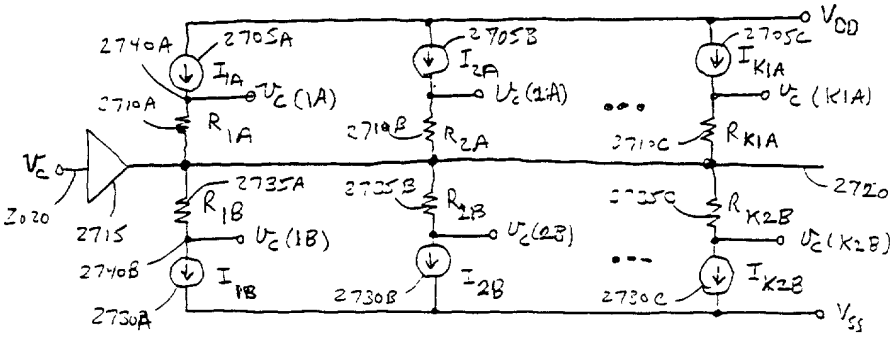


FIG. 27

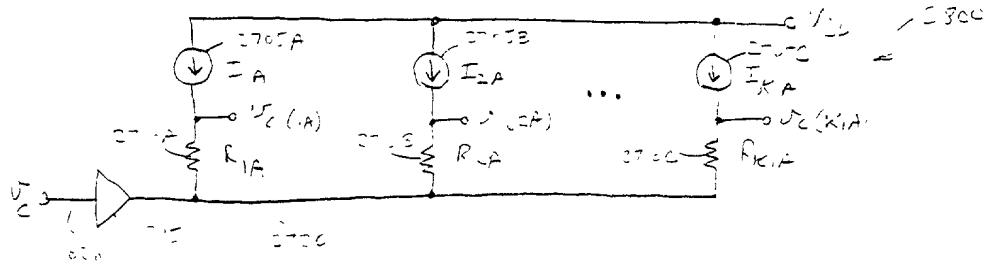


FIG. 28

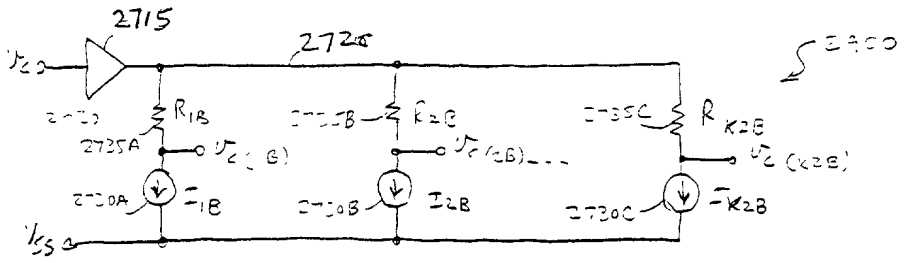


FIG. 29

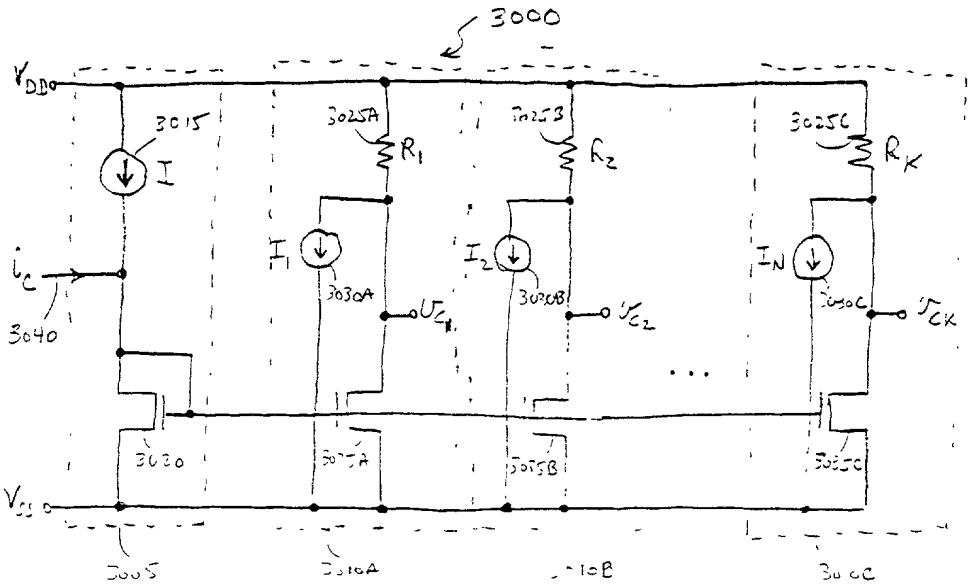

3000
V_{DD}
3015
I
i_C
3040
3025A
R_1
I_1
3030A
U_{C1}
3025B
R_2
I_2
3030B
U_{C2}
3025C
R_K
I_N
3030C
U_{CK}
3020
3010A
3010B
3010C
V_{SS}
3005
3010A
3010B
3010C

FIG. 3C

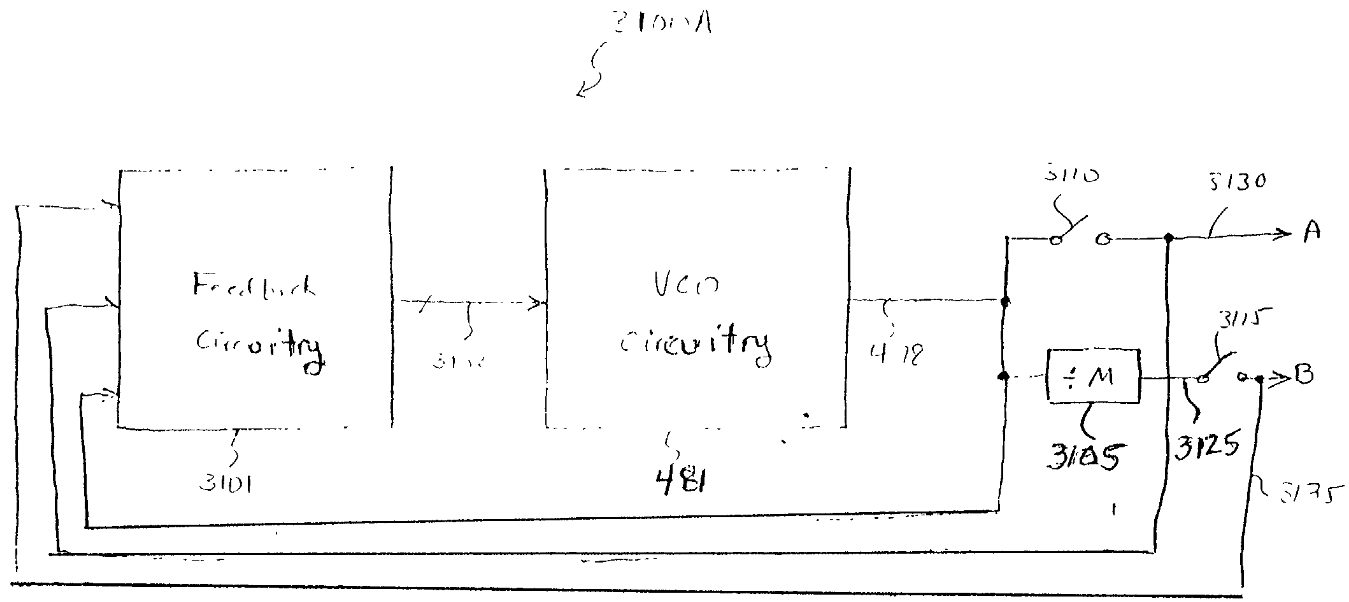

3100A
Feedback Circuitry
3101
VCO Circuitry
481
418
3110
3130
A
÷ M
3105
3115
B
3125
3135

FIG. 31A

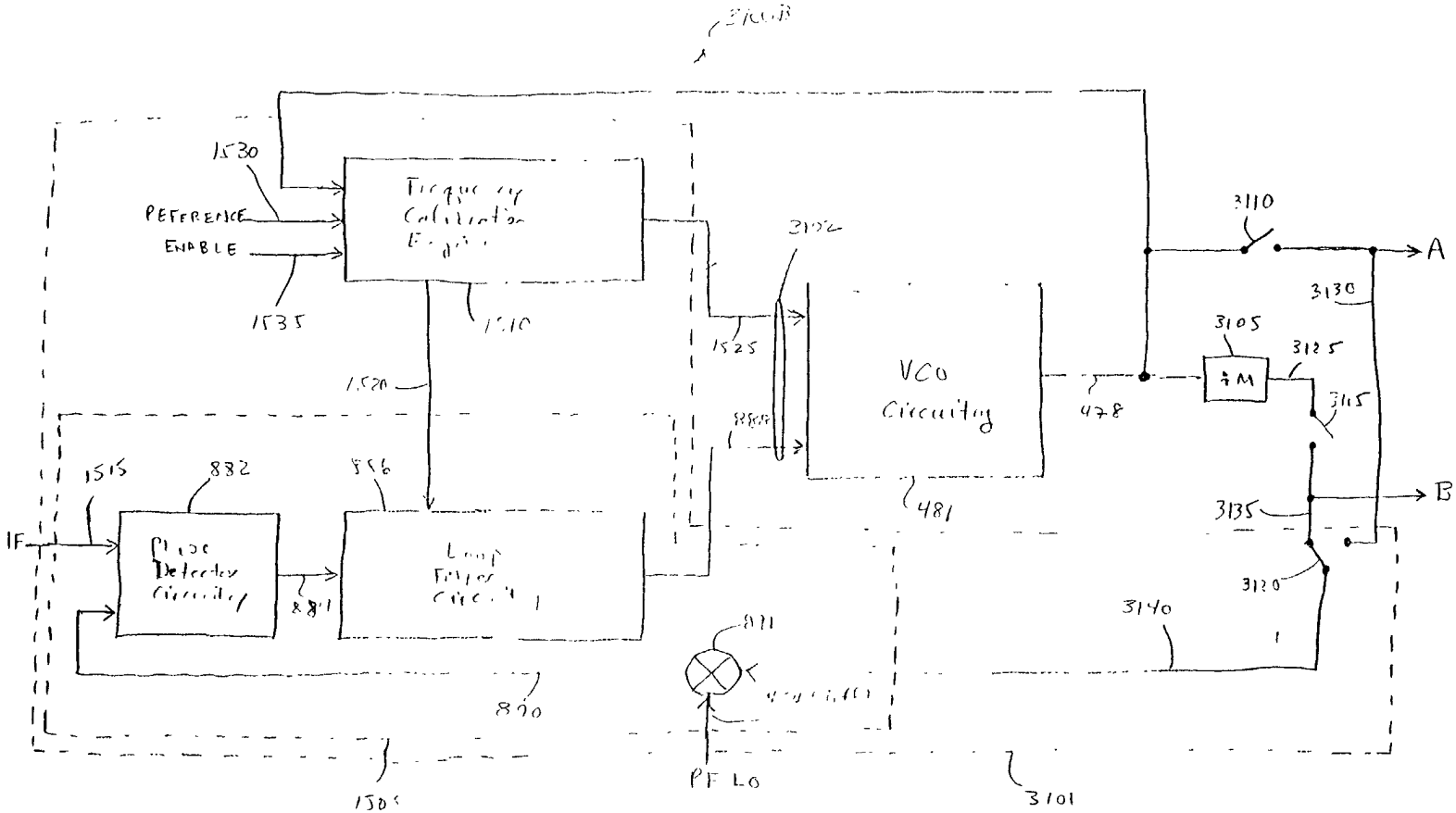

1530
REFERENCE
ENABLE
1535
1510
1520
1525
3102
VCO Circuitry
481
478
3110
A
3130
3105
÷M
3125
3115
B
3135
3120
3140
1515
882
IF
Phase Detector Circuitry
881
884
Loop Filter Circuitry
890
871
PF LO
1505
3101

FIG. 31B

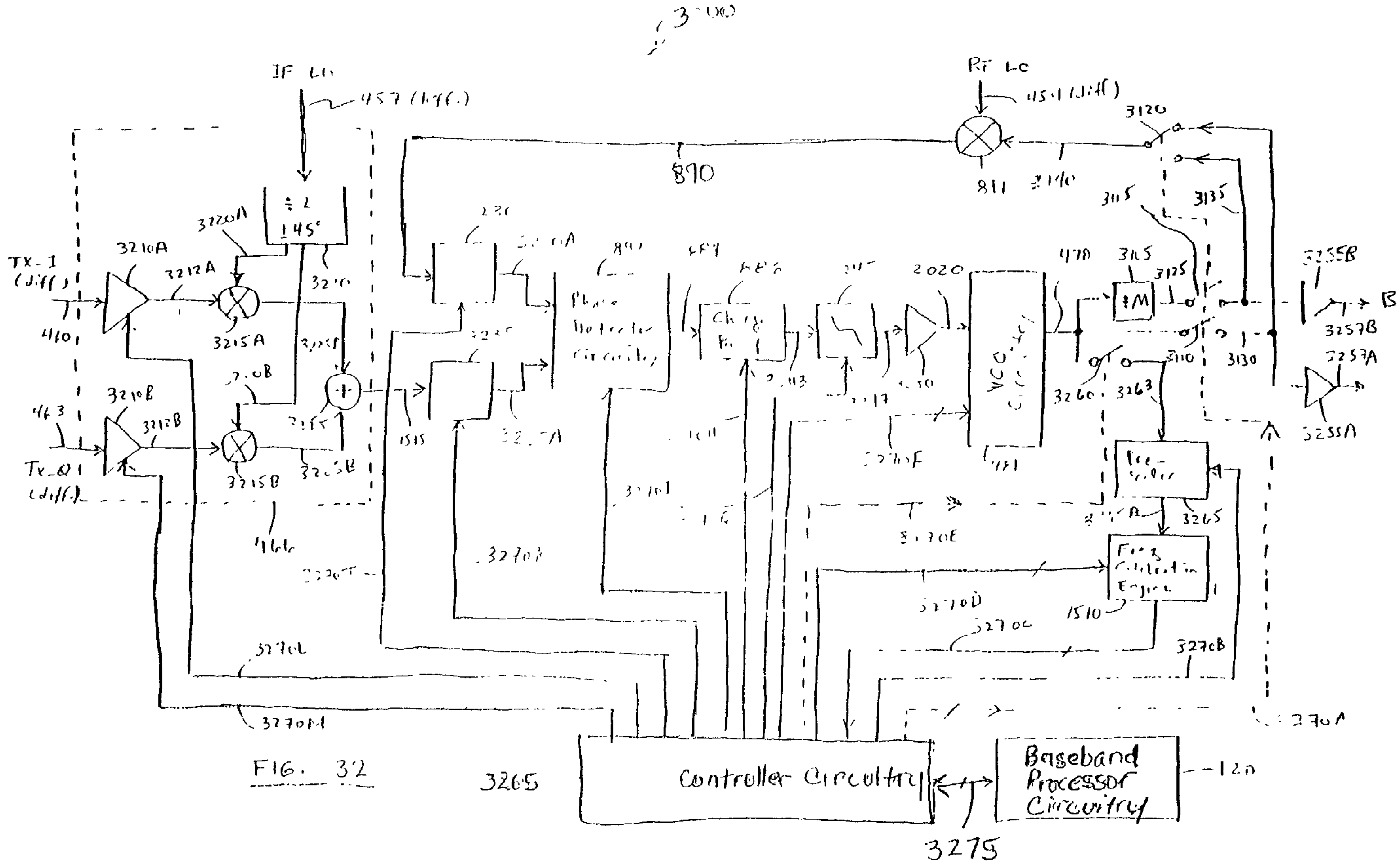

IF LO
RF LO
890
811
TX-I (diff)
Tx-Q (diff)
3210A
3210B
3215A
3215B
3212A
3220A
Controller Circuitry
Baseband Processor Circuitry
3275
3265
1510
3257B
3257A
3255B
3255A
B
3120
3130
3135
2020
3260
3263
3270M
3270D
3270B
3270A

FIG. 32

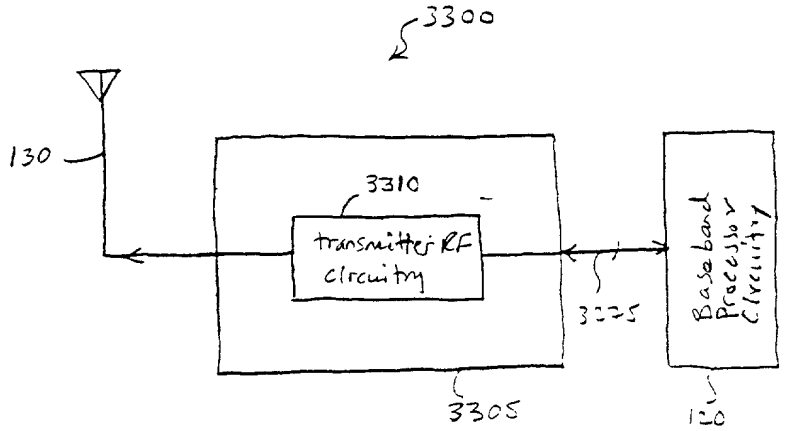


FIG. 33

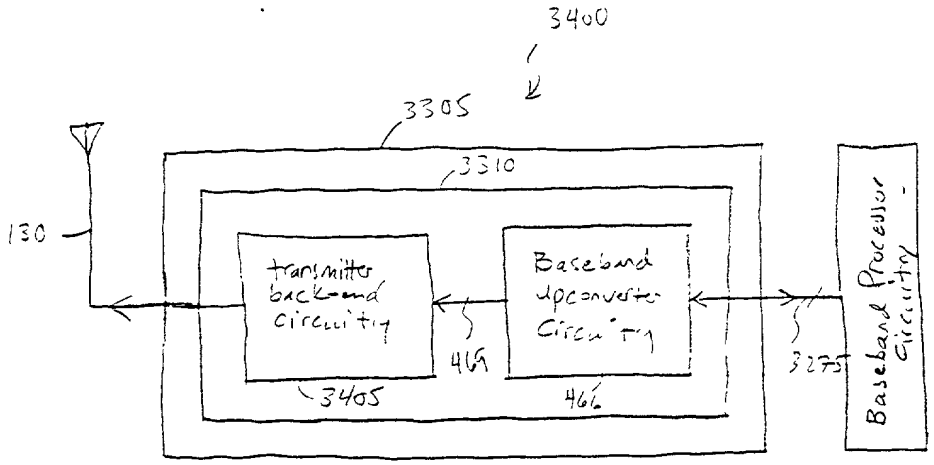


FIG. 34

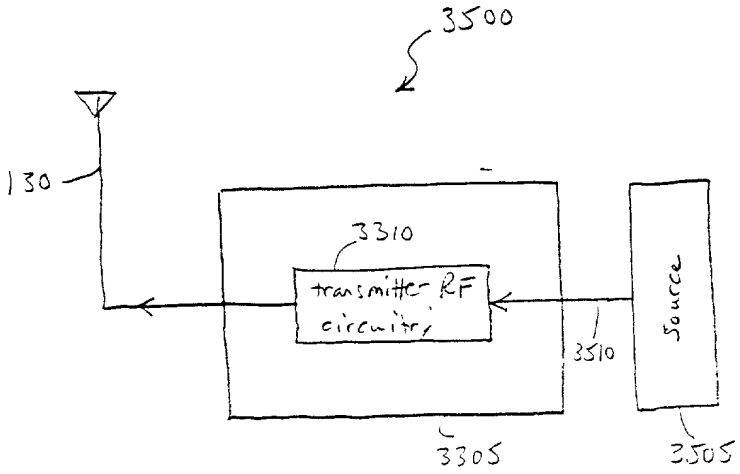

3500
130
3310
transmitter RF circuitry
3510
source
3305
3505

FIG. 35